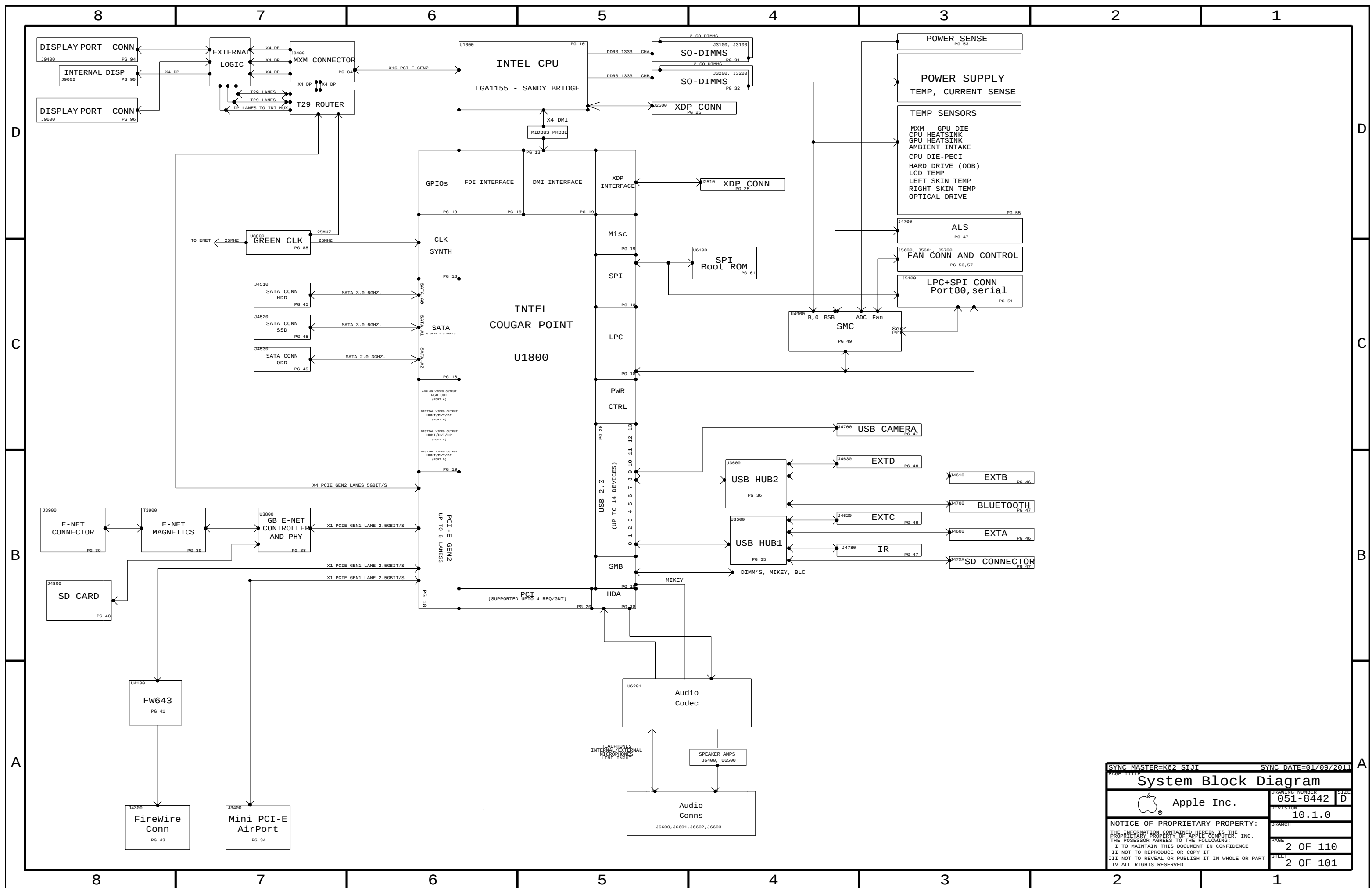
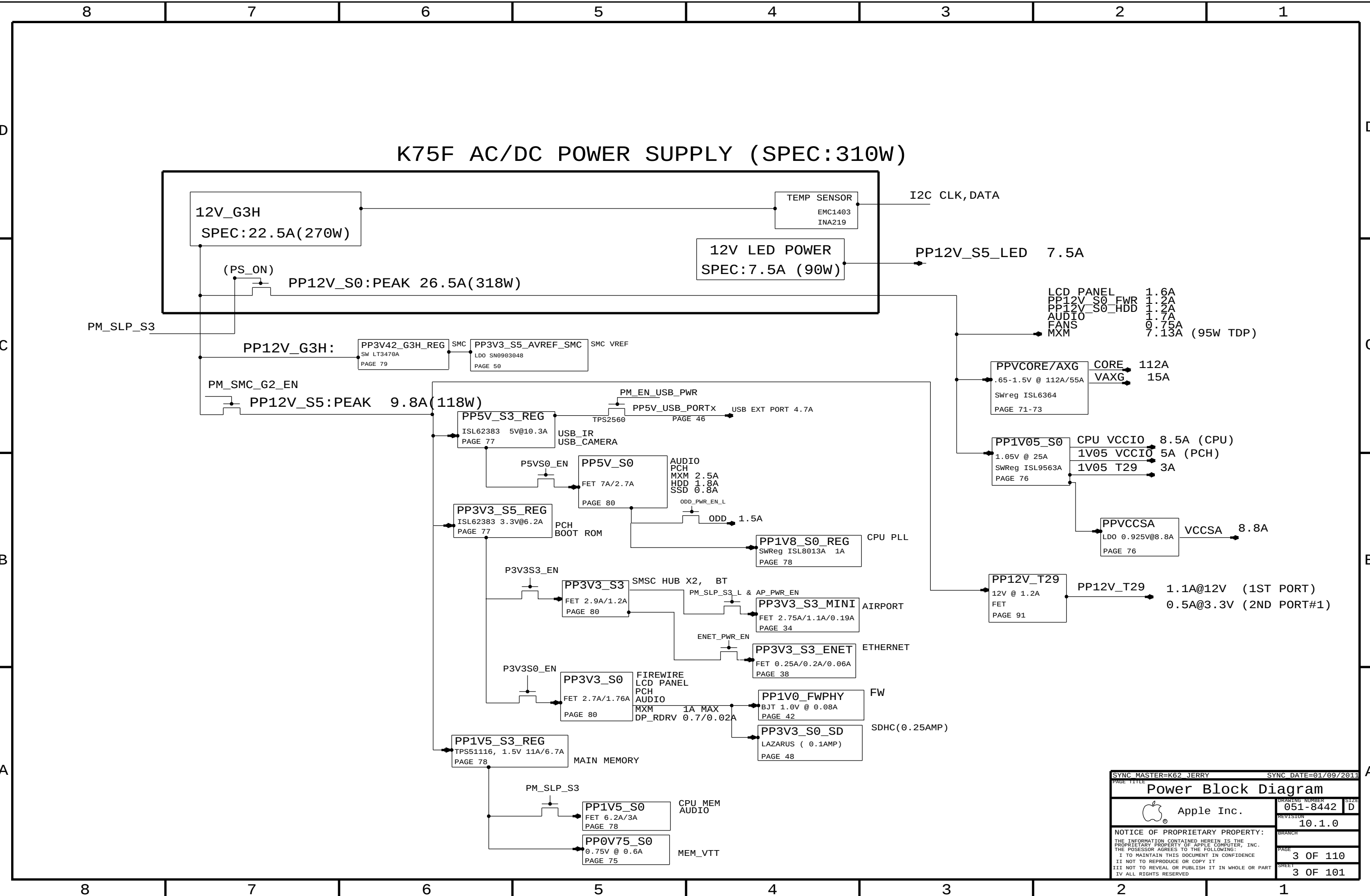


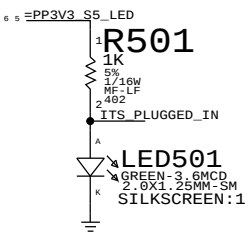




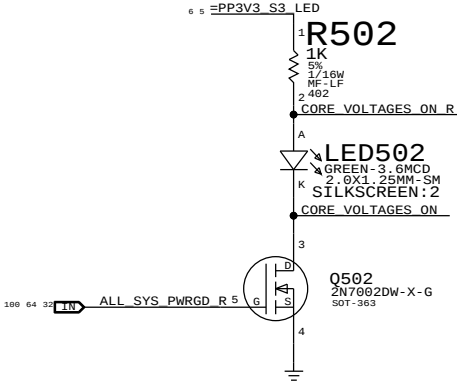
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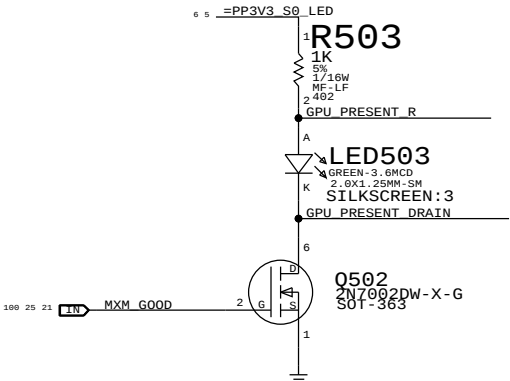
S5 Led



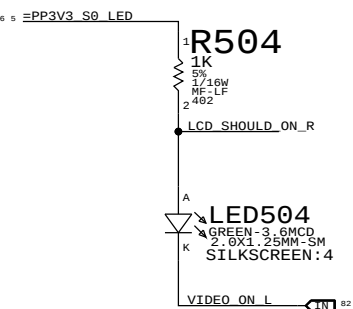
ALL_SYS_PWRGD Led



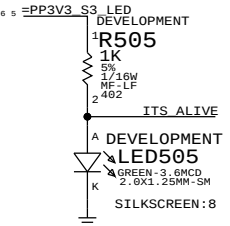
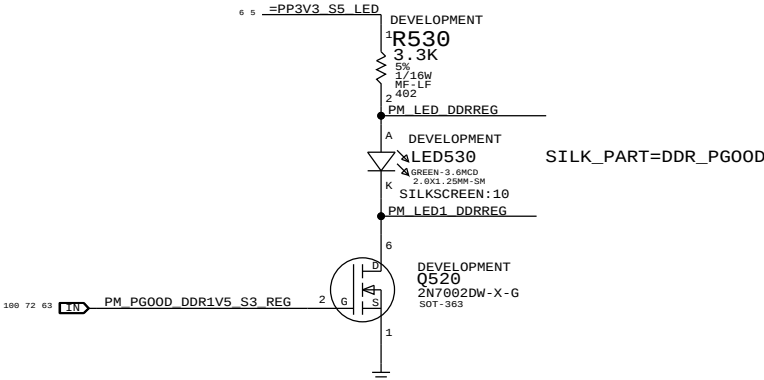
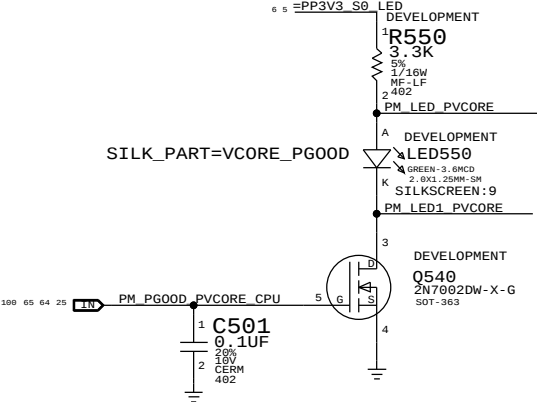
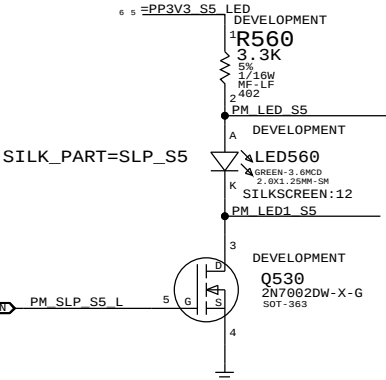
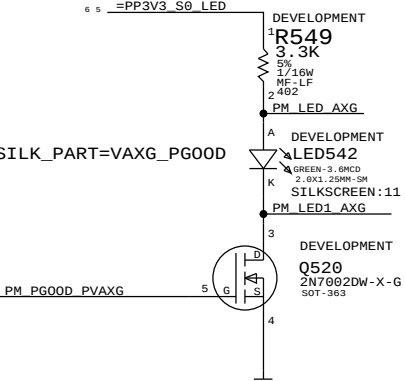
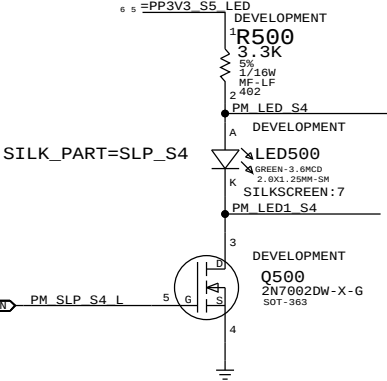
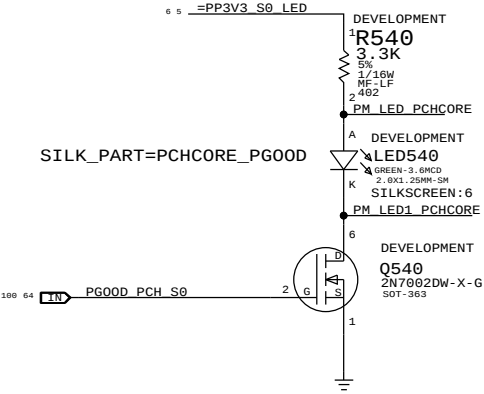
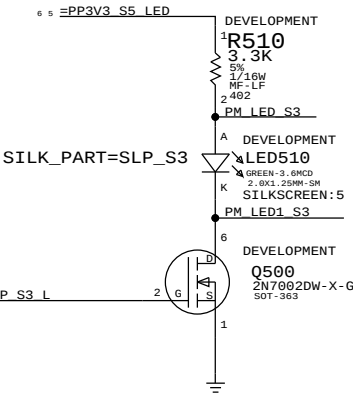
MXM PWR GOOD Led



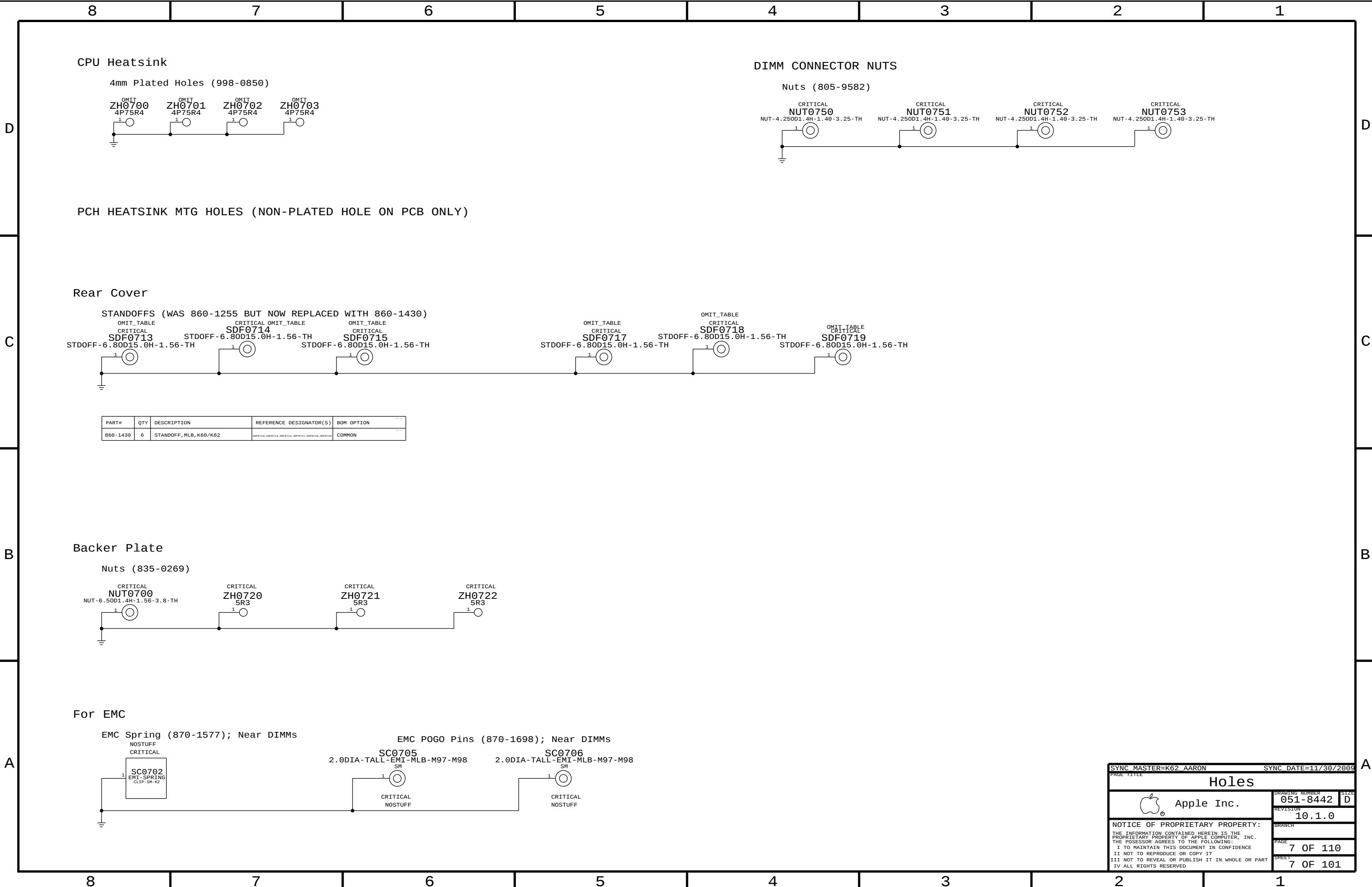
VIDEO ON Led



PROTO DEBUG LEDS ARE SHOWN BELOW

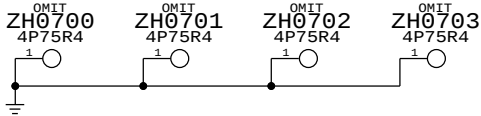


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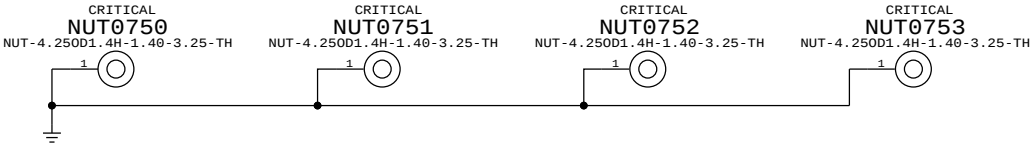
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK MTG HOLES (NON-PLATED HOLE ON PCB ONLY)

Rear Cover

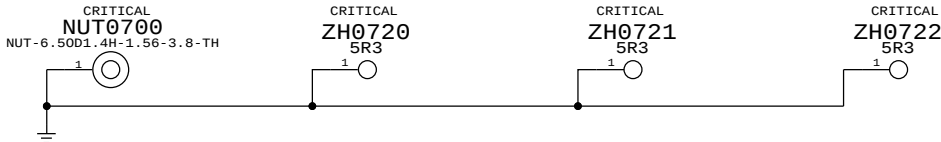
STANDOFFS (WAS 860-1255 BUT NOW REPLACED WITH 860-1430)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-1430	6	STANDOFF, MLB, K60/K62	SDF0713, SDF0714, SDF0715, SDF0717, SDF0718, SDF0719	COMMON

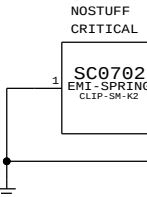
Backer Plate

Nuts (835-0269)

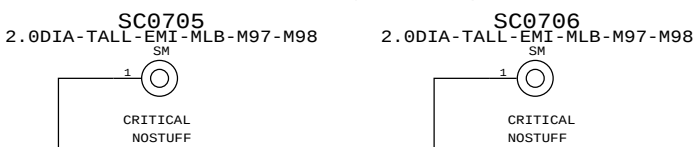


For EMC

EMC Spring (870-1577); Near DIMMs



EMC POGO Pins (870-1698); Near DIMMs



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		PAGE	7 OF 110
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UNUSED CPU SIGNALS		NC ON UNUSED PCIE ALIASES		NC ON UNUSED DISPLAY ALIASES		NC ON UNUSED FDI ALIASES			
19 TP_CPU_RSVD<16..1> == NC_CPU_RSVD<16..1> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CPU_RSVD<46..19> == NC_CPU_RSVD<46..19> MAKE_BASE=TRUE NO_TEST=TRUE		18 TP_PCIE_CLK100M_PE5P == NC_PCIE_CLK100M_PE5P MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCIE_CLK100M_PE5N == NC_PCIE_CLK100M_PE5N MAKE_BASE=TRUE NO_TEST=TRUE 21 TP_PCIE_CLK100M_PE6P == NC_PCIE_CLK100M_PE6P MAKE_BASE=TRUE NO_TEST=TRUE 21 TP_PCIE_CLK100M_PE6N == NC_PCIE_CLK100M_PE6N MAKE_BASE=TRUE NO_TEST=TRUE 21 TP_PCIE_CLK100M_PE7P == NC_PCIE_CLK100M_PE7P MAKE_BASE=TRUE NO_TEST=TRUE 21 TP_PCIE_CLK100M_PE7N == NC_PCIE_CLK100M_PE7N MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PE_RX_N<3..0> == NC_PE_RXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PE_RX_P<3..0> == NC_PE_RXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PE_TX_N<3..0> == NC_PE_TXN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PE_TX_P<3..0> == NC_PE_TXP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCIE_D2R_PERN4 == NC_PCIE_D2R_PERN4 MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCIE_D2R_PERP4 == NC_PCIE_D2R_PERP4 MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCIE_R2D_PETN4 == NC_PCIE_R2D_PETN4 MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCIE_R2D_PETP4 == NC_PCIE_R2D_PETP4 MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PCIE_CLK100M_PE4P == NC_PCIE_CLK100M_PE4P MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_PCIE_CLK100M_PE4N == NC_PCIE_CLK100M_PE4N MAKE_BASE=TRUE NO_TEST=TRUE		19 TP_CRT_IG_DDC_CLK == NC_CRT_IG_DDC_CLK MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_DDC_DATA == NC_CRT_IG_DDC_DATA MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_RED == NC_CRT_IG_RED MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_GREEN == NC_CRT_IG_GREEN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_BLUE == NC_CRT_IG_BLUE MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_HSYNC == NC_CRT_IG_HSYNC MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_CRT_IG_VSYNC == NC_CRT_IG_VSYNC MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_MLN<3..0> == NC_DP_IG_B_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_MLP<3..0> == NC_DP_IG_B_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_AUX_N == NC_DP_IG_B_AUXN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_AUX_P == NC_DP_IG_B_AUXP MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_HPD == NC_DP_IG_B_HPD MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_DDC_CLK == NC_DP_IG_B_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_B_DDC_DATA == NC_DP_IG_B_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_MLN<3..0> == NC_DP_IG_C_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_MLP<3..0> == NC_DP_IG_C_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_AUX_N == NC_DP_IG_C_AUXN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_AUX_P == NC_DP_IG_C_AUXP MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_HPD == NC_DP_IG_C_HPD MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_CTRL_CLK == NC_DP_IG_C_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_C_CTRL_DATA == NC_DP_IG_C_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_MLN<3..0> == NC_DP_IG_D_MLN<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_MLP<3..0> == NC_DP_IG_D_MLP<3..0> MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_AUXN == NC_DP_IG_D_AUXN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_AUXP == NC_DP_IG_D_AUXP MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_HPD == NC_DP_IG_D_HPD MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_CTRL_CLK == NC_DP_IG_D_CTRL_CLK MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_DP_IG_D_CTRL_DATA == NC_DP_IG_D_CTRL_DATA MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_TVCLKINN == NC_SDVO_TVCLKINN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_TVCLKINP == NC_SDVO_TVCLKINP MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_STALLN == NC_SDVO_STALLN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_STALLP == NC_SDVO_STALLP MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_INTN == NC_SDVO_INTN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SDVO_INTP == NC_SDVO_INTP MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCH_L_BKLTCTL == NC_PCH_L_BKLTCTL MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCH_L_BKLTEN == NC_PCH_L_BKLTEN MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCH_L_VDD_EN == NC_PCH_L_VDD_EN MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCH_CLKOUT_DPN == NC_PCH_CLKOUT_DPN MAKE_BASE=TRUE NO_TEST=TRUE 18 TP_PCH_CLKOUT_DPP == NC_PCH_CLKOUT_DPP MAKE_BASE=TRUE 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NC_SATA_F_R2D_CN MAKE_BASE=TRUE NO_TEST=TRUE 19 TP_SATA_F_R2D_CP == NC_SATA_F_R2D_CP MAKE_BASE=TRUE NO_TEST=TRUE		NC ON UNUSED SATA ALIASES	
NC ON UNUSED PCI ALIASES		NC ON UNUSED USB ALIASES							
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NC ON UNUSED MEM ALIASES									
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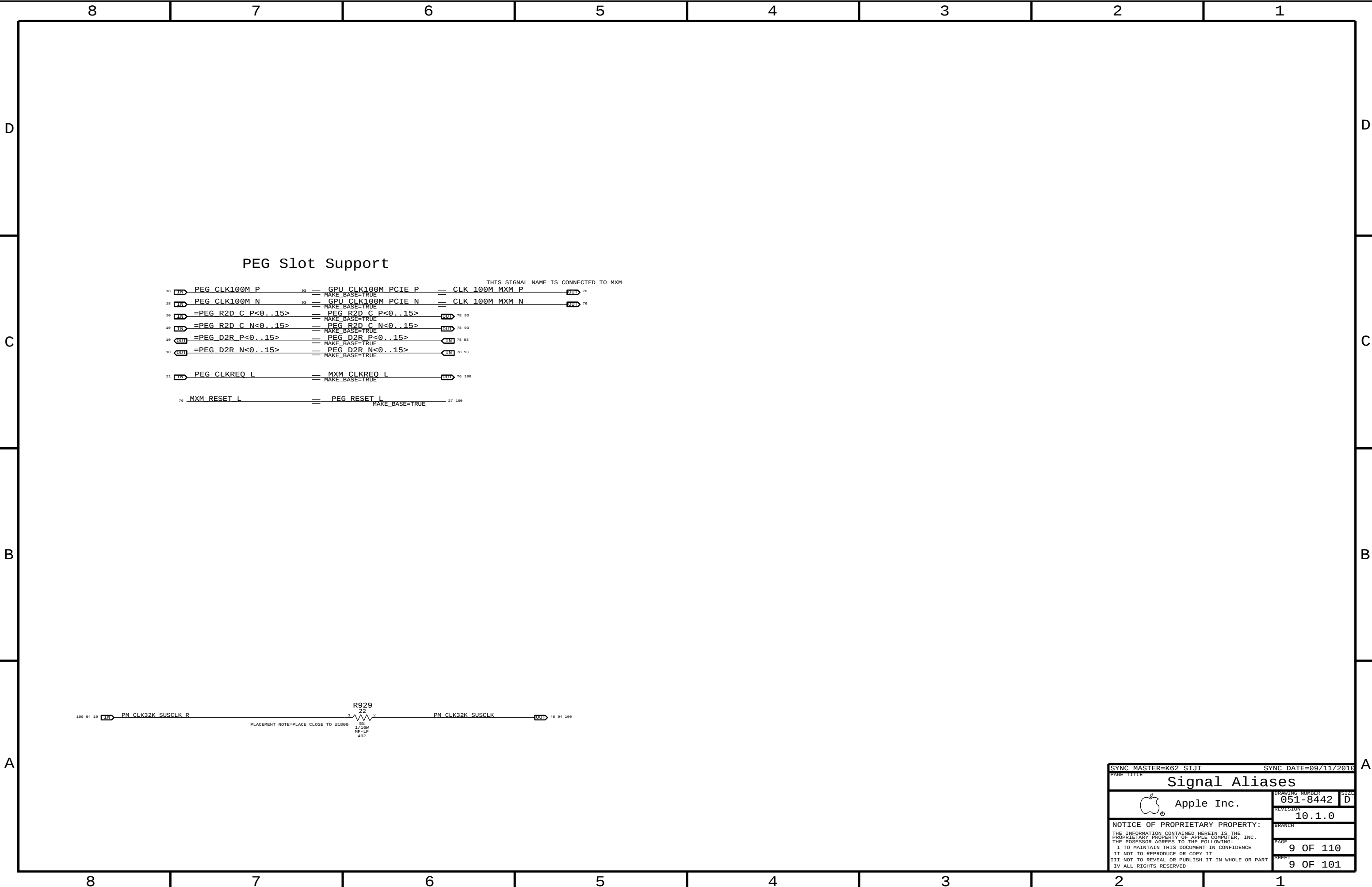
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SYNC_DATE=09/11/2016

PAGE TITLE

Signal Aliases

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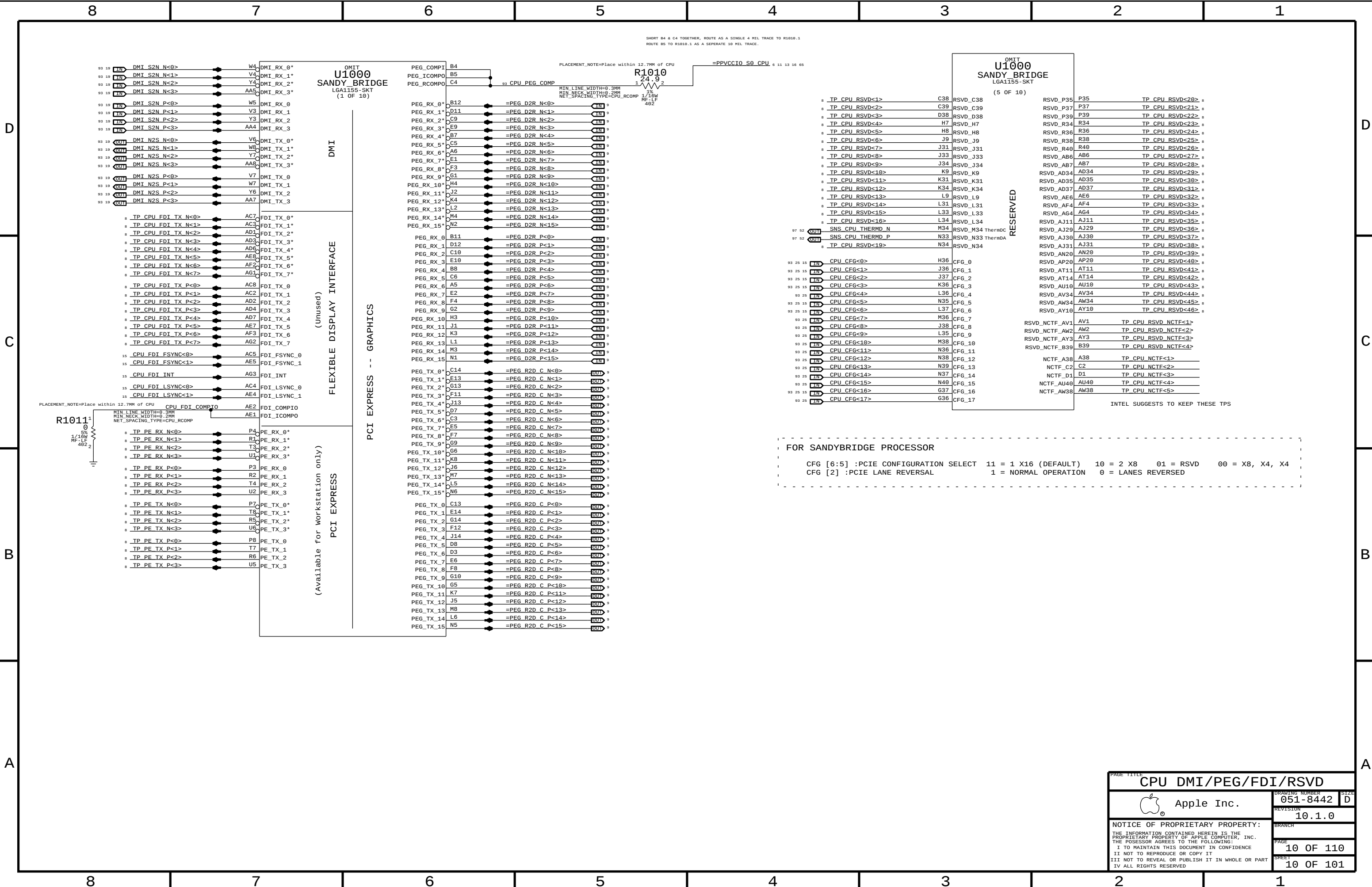
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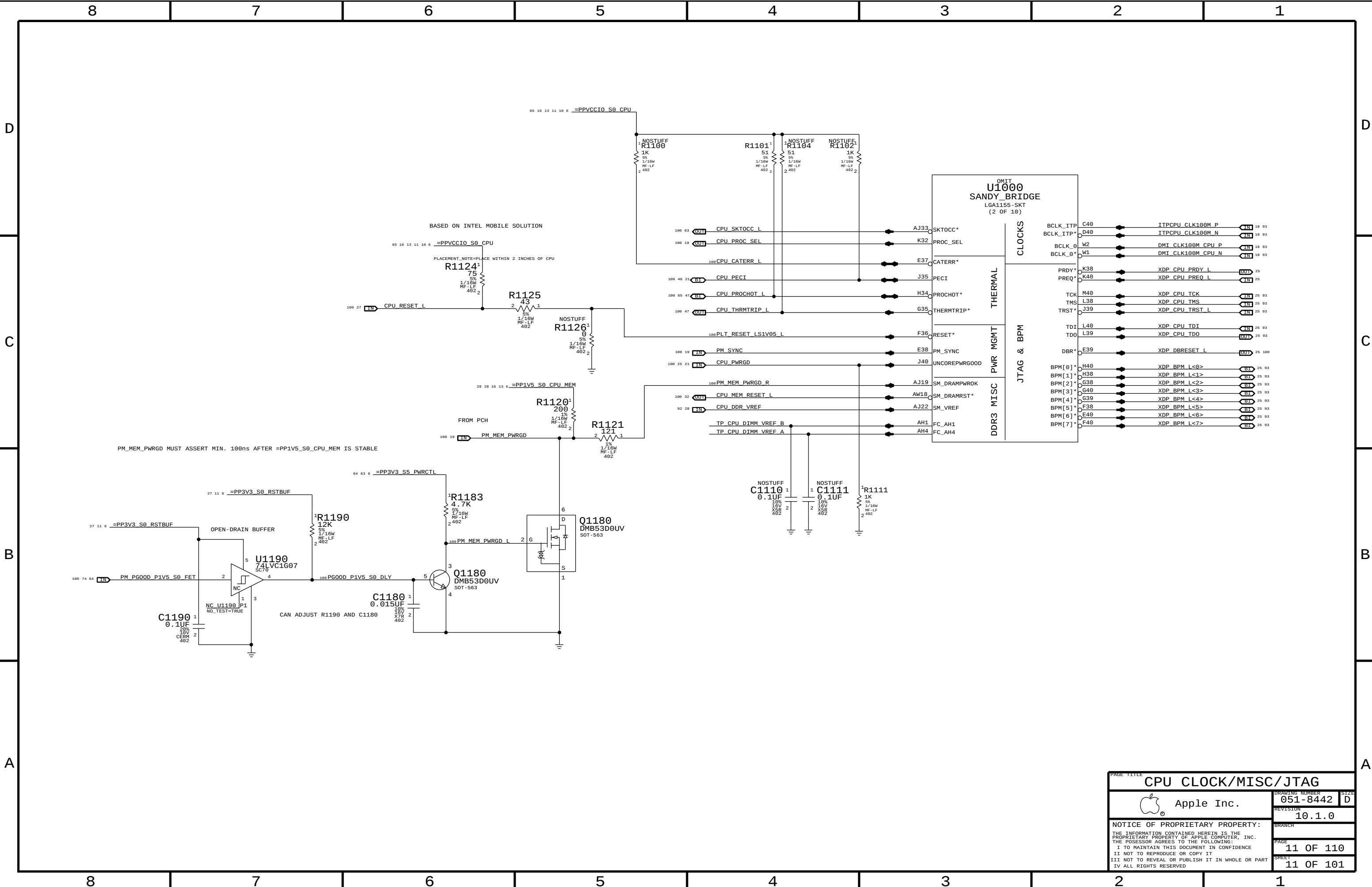
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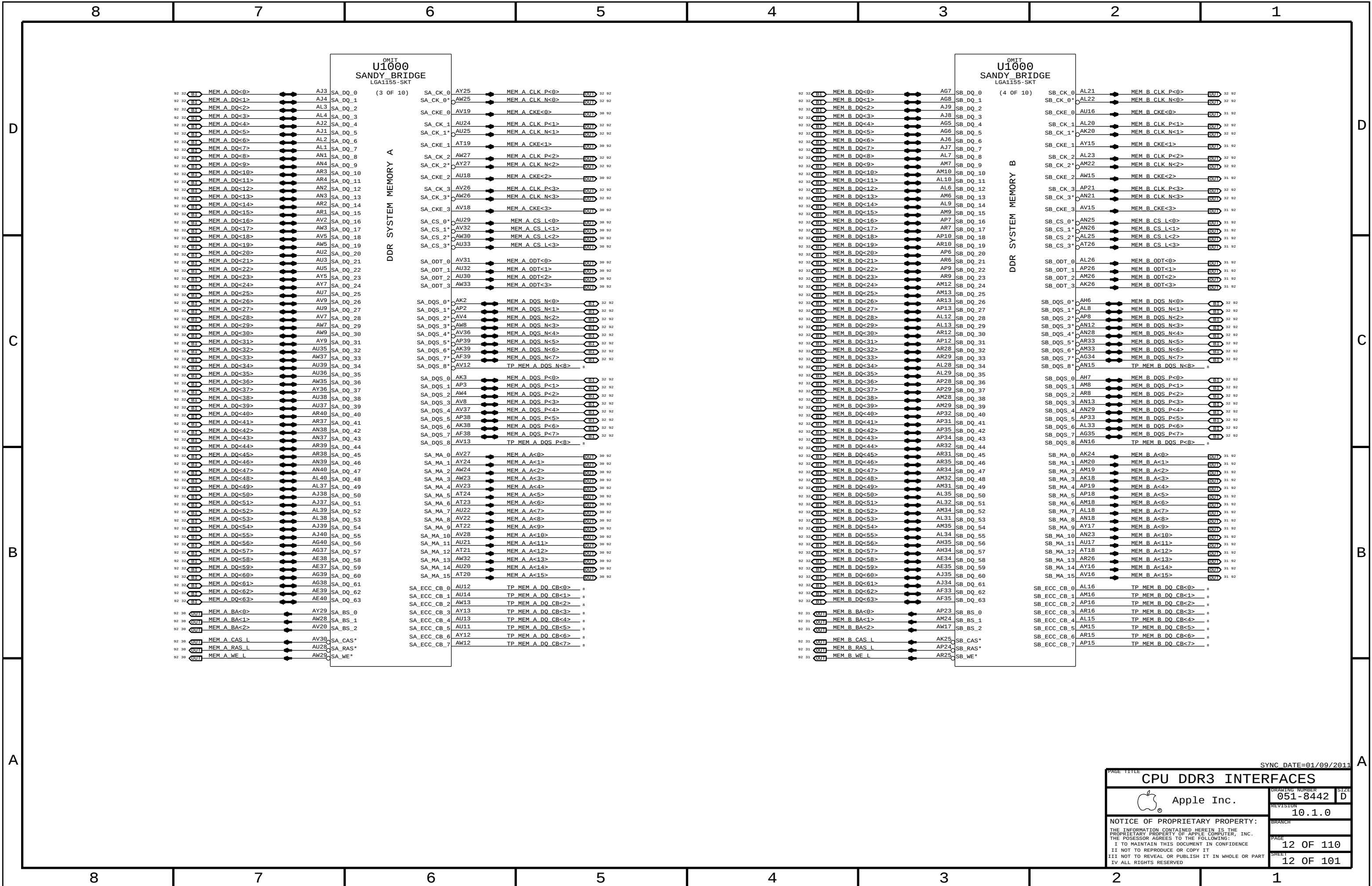
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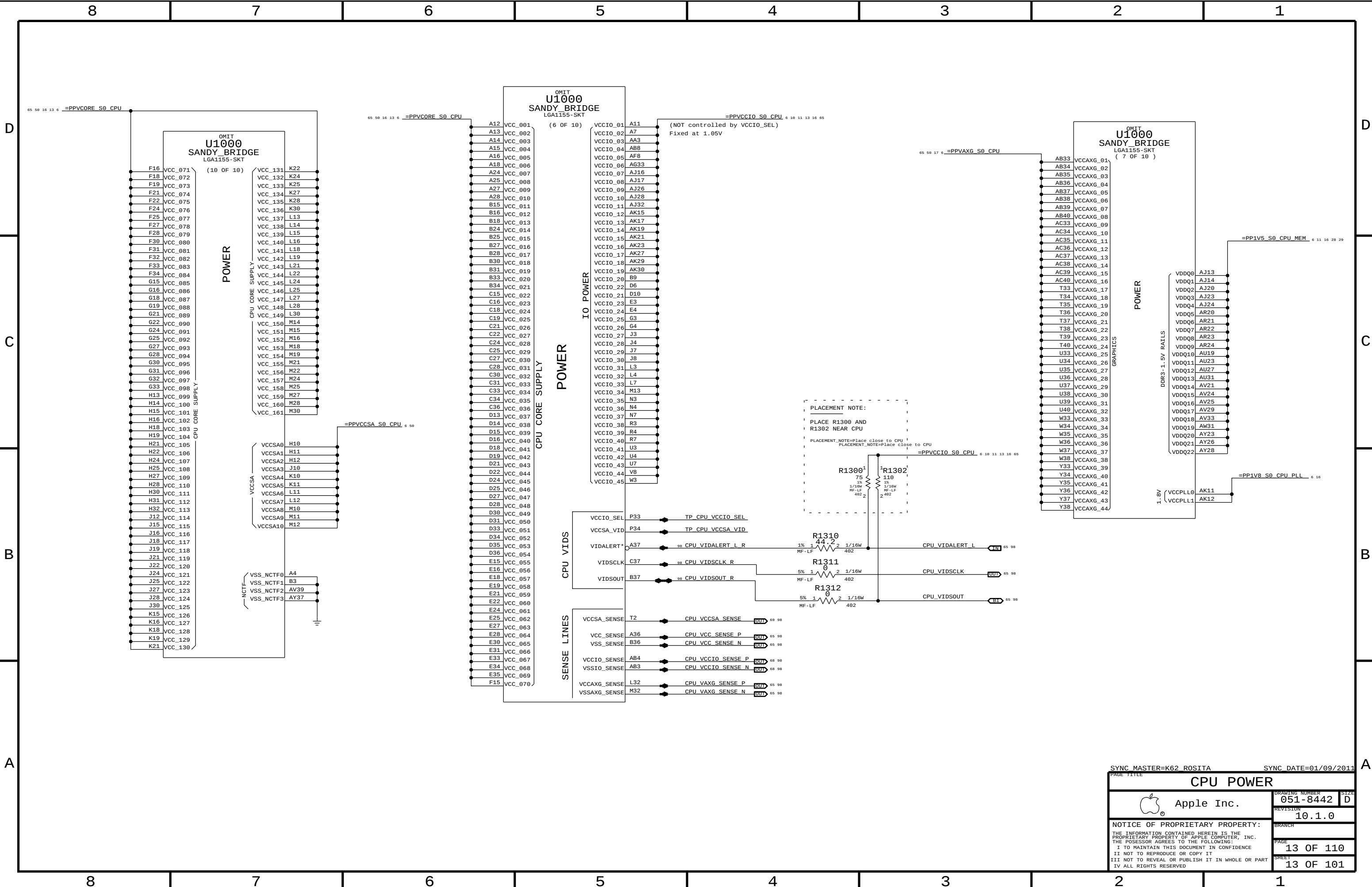
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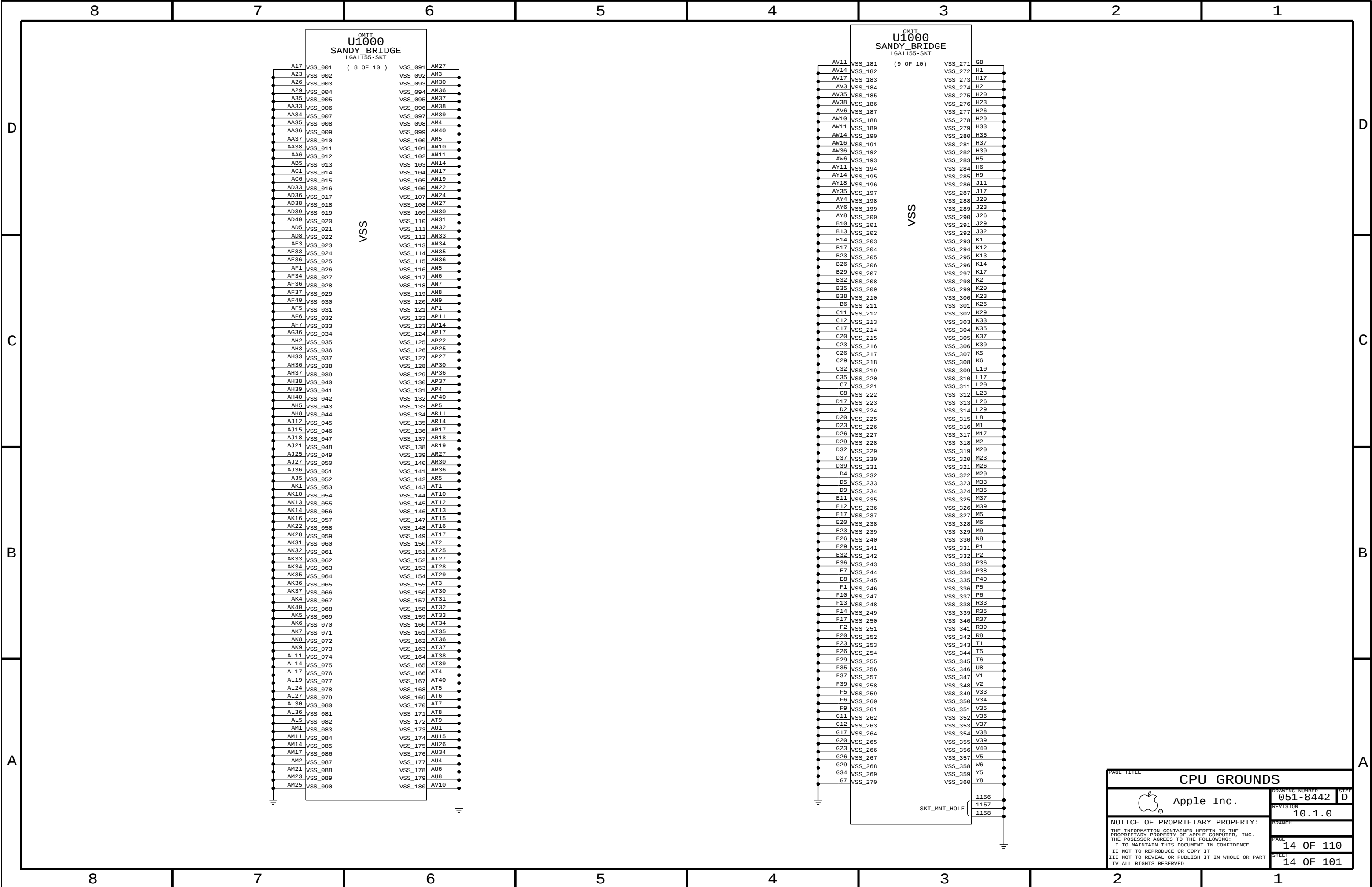
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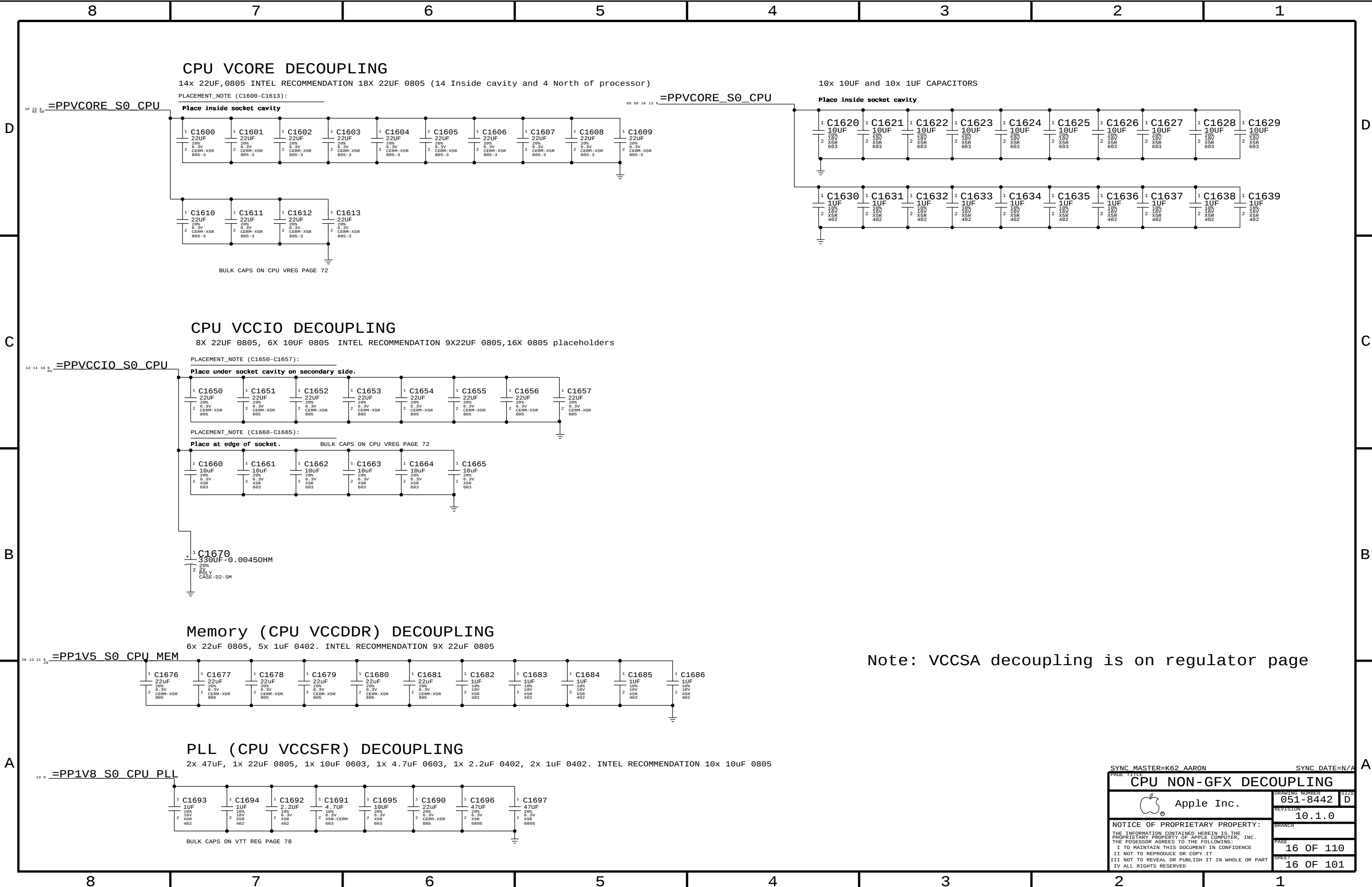












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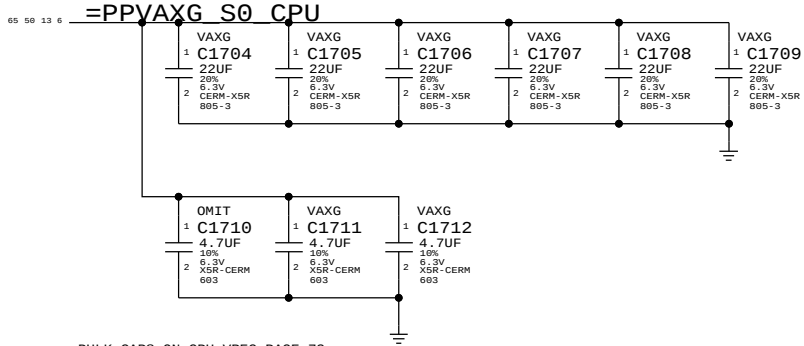
CPU NON-GFX DECOUPLING		
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VAXG DECOUPLING

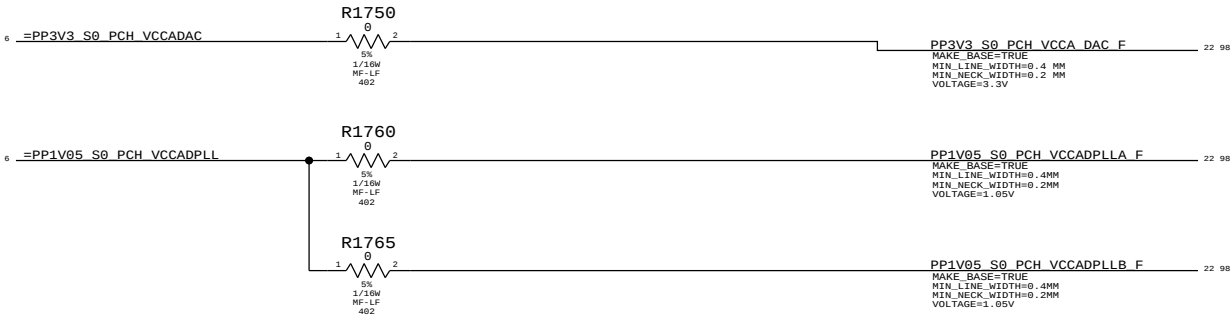
INTEL RECOMMENDATION 6X22UF 0805,3X 4.7UF

PLACEMENT_NOTE (C1704-C1709):

Place inside socket cavity

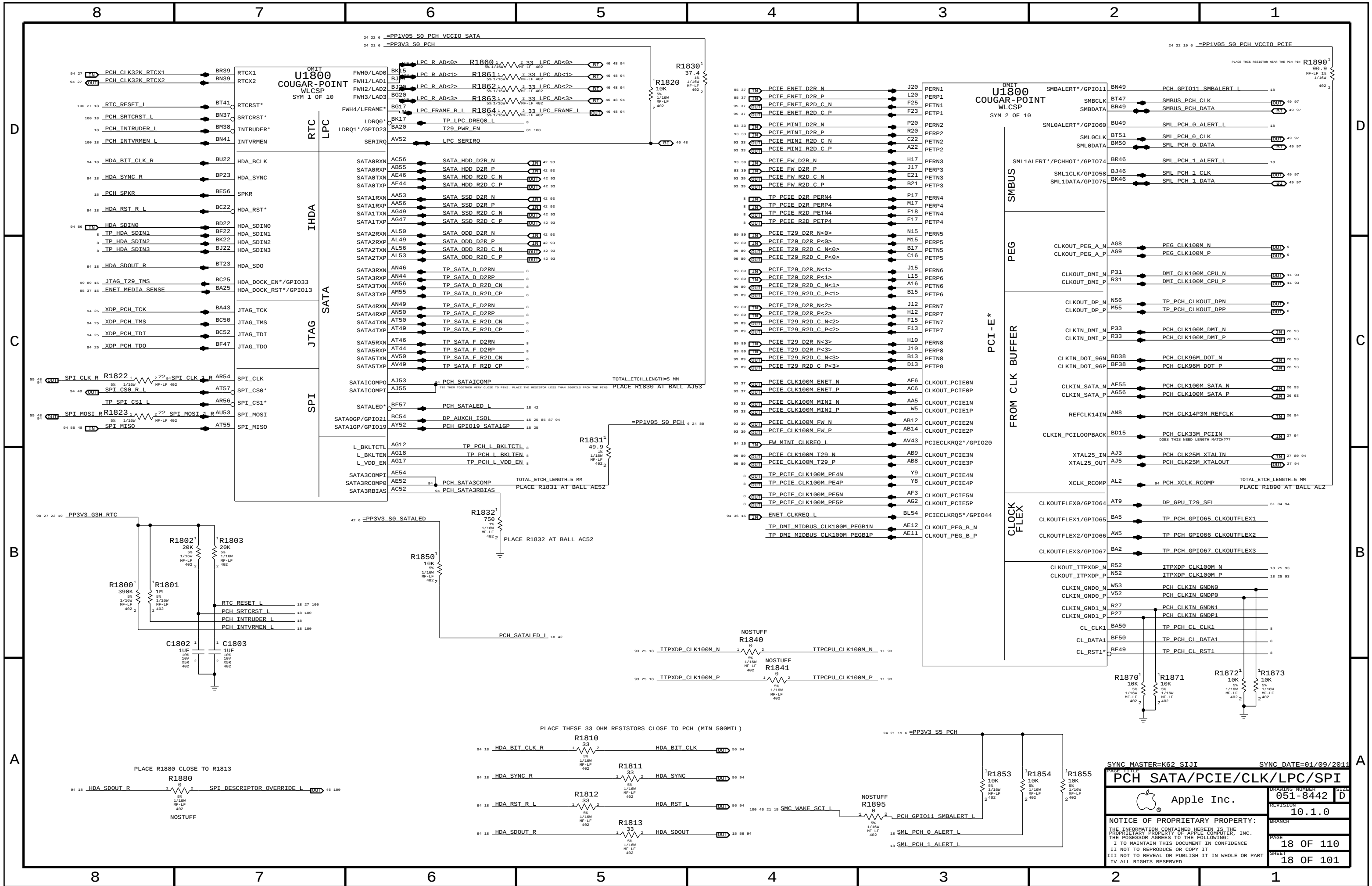


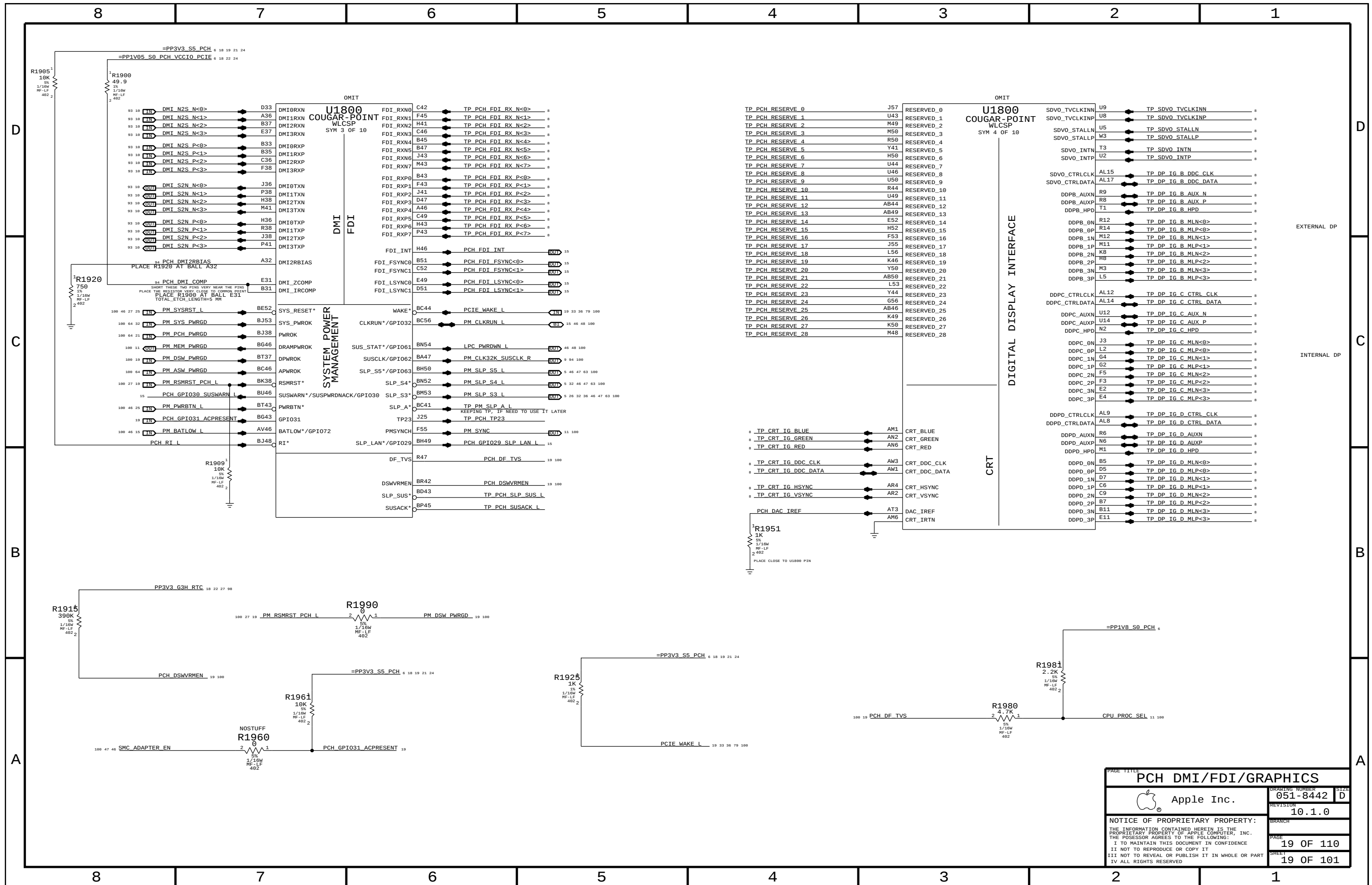
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0586	1	CAP, 4.7UF, 10%, 6.3V, 0603	C1710	VAXG
113S0022	1	RES, 0 OHM, 5%, 0603	C1710	NO_VAXG

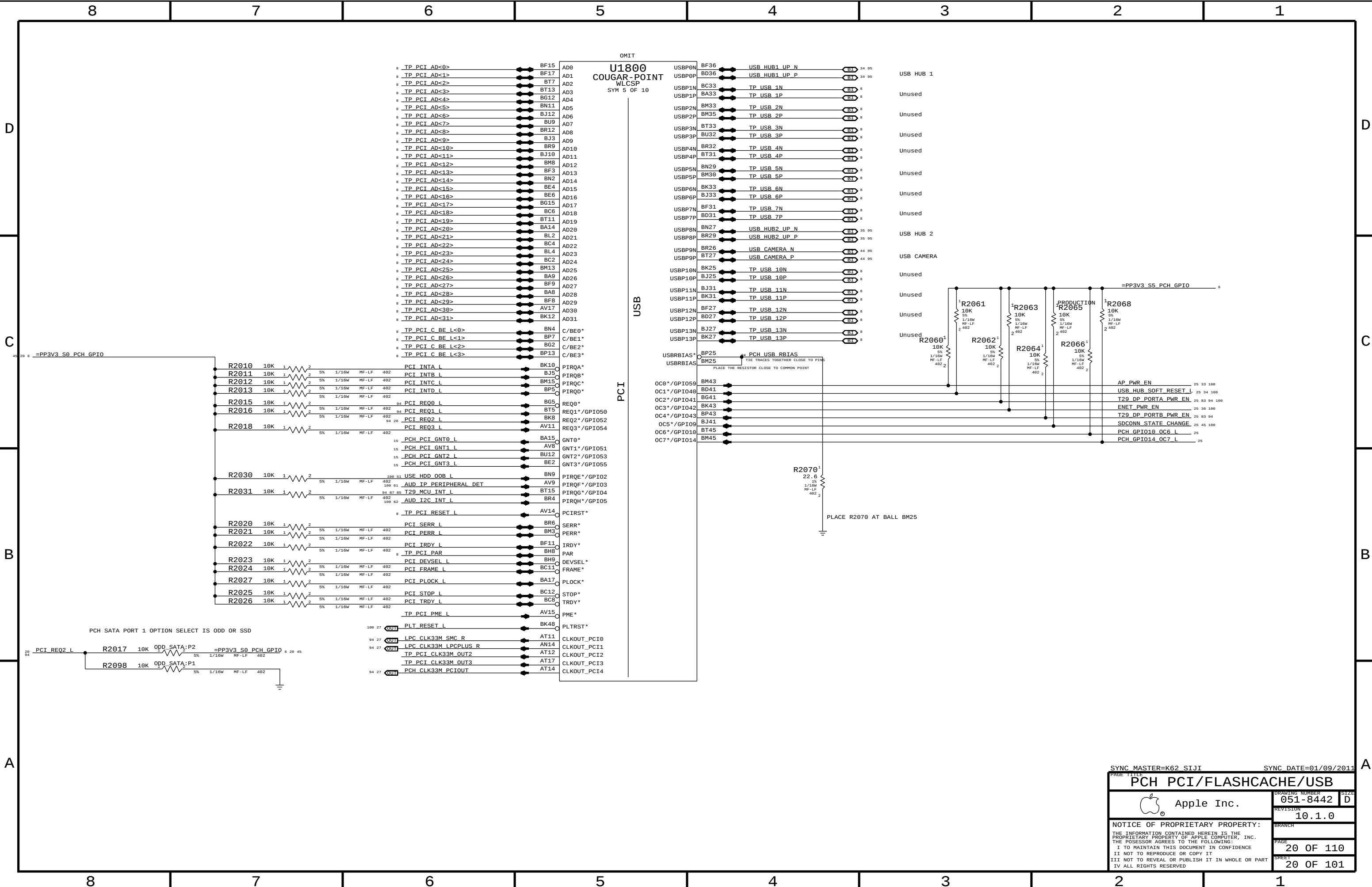


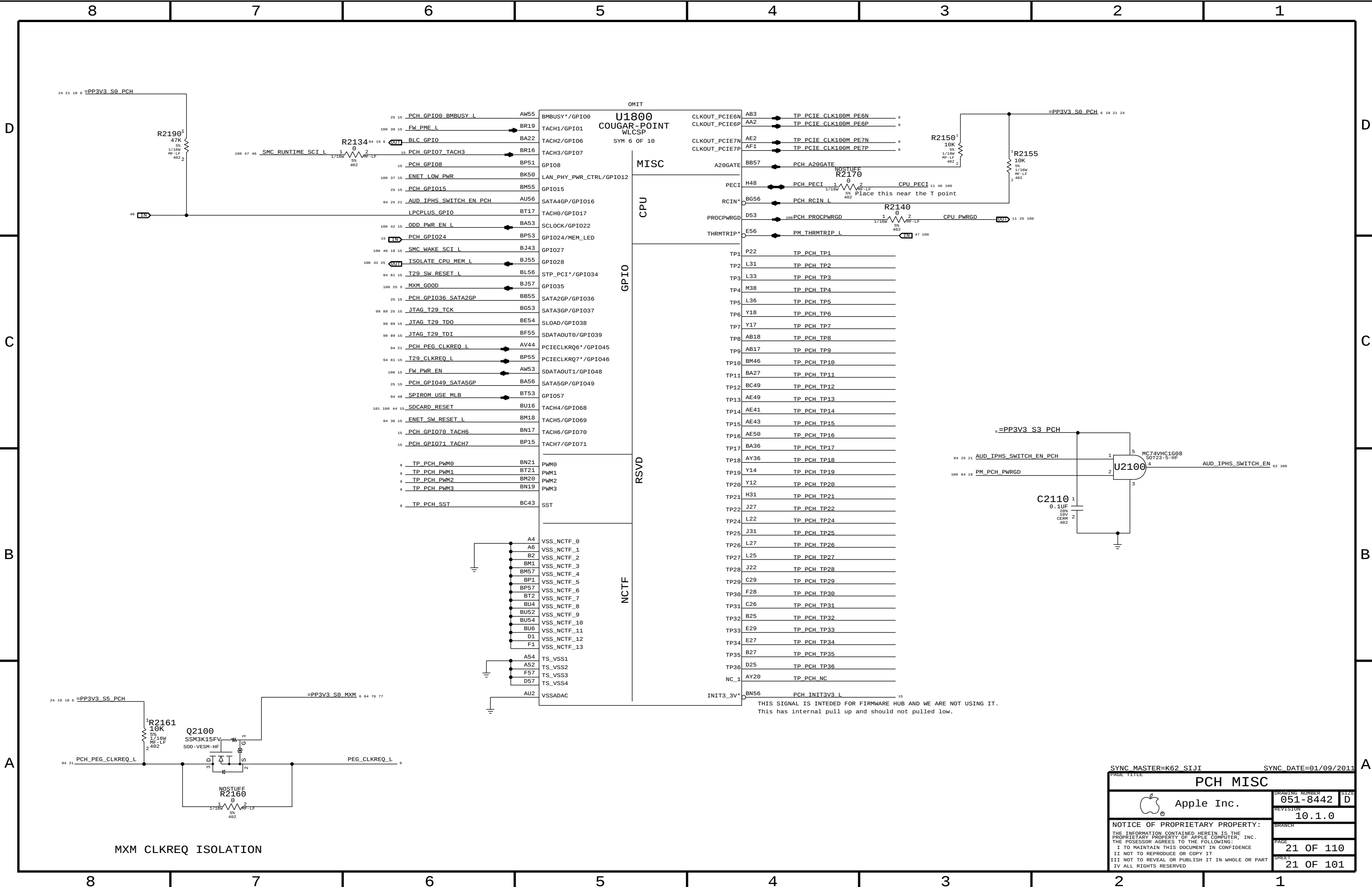
SYNC MASTER=K62 AARON SYNC DATE=11/30/2009

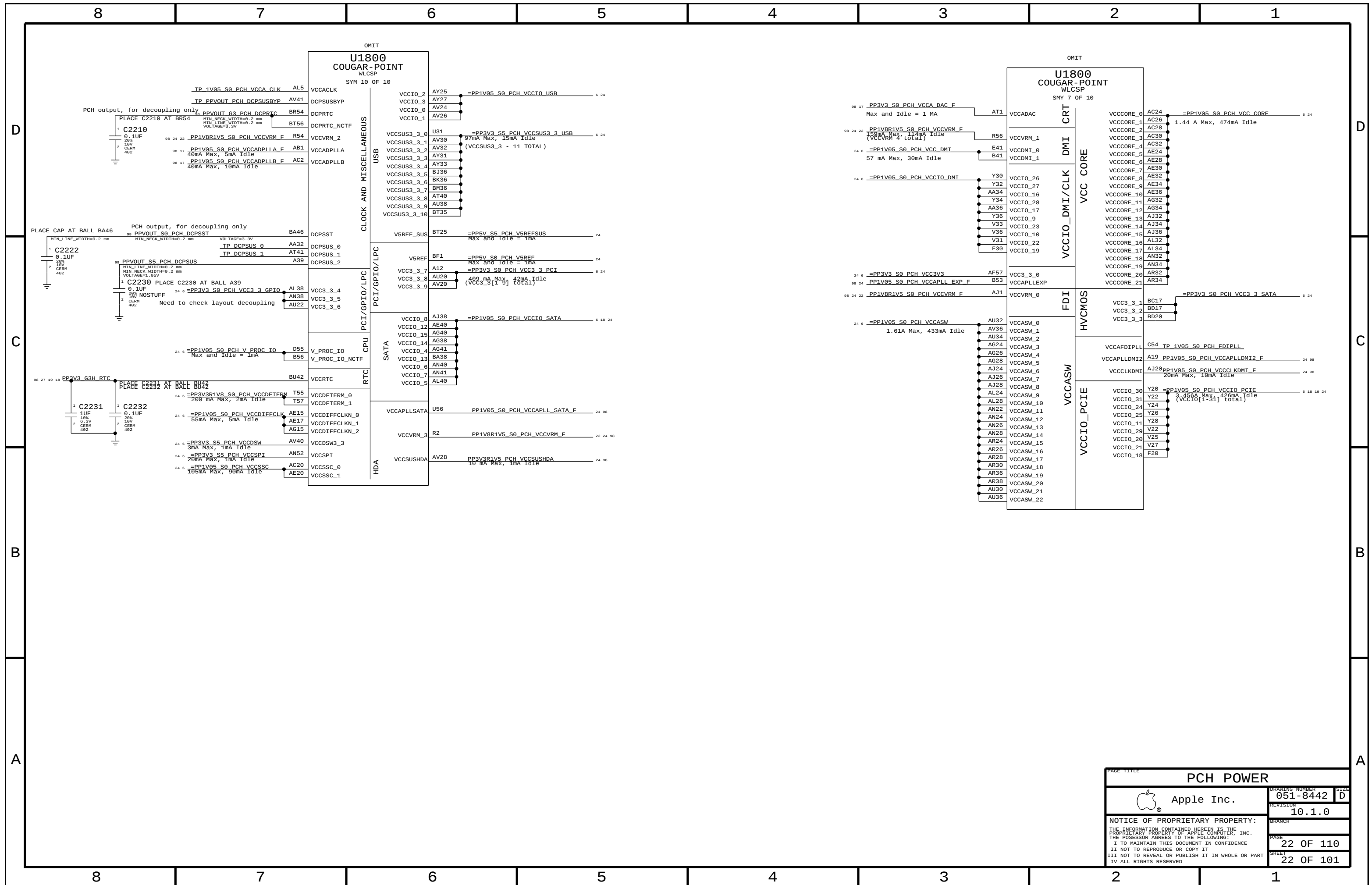
PAGE TITLE		DRAWING NUMBER		SIZE
GFX DECOUPLING & PCH PWR ALIAS		051-8442		D
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		BRANCH		
		PAGE		17 OF 110
		SHEET		17 OF 101

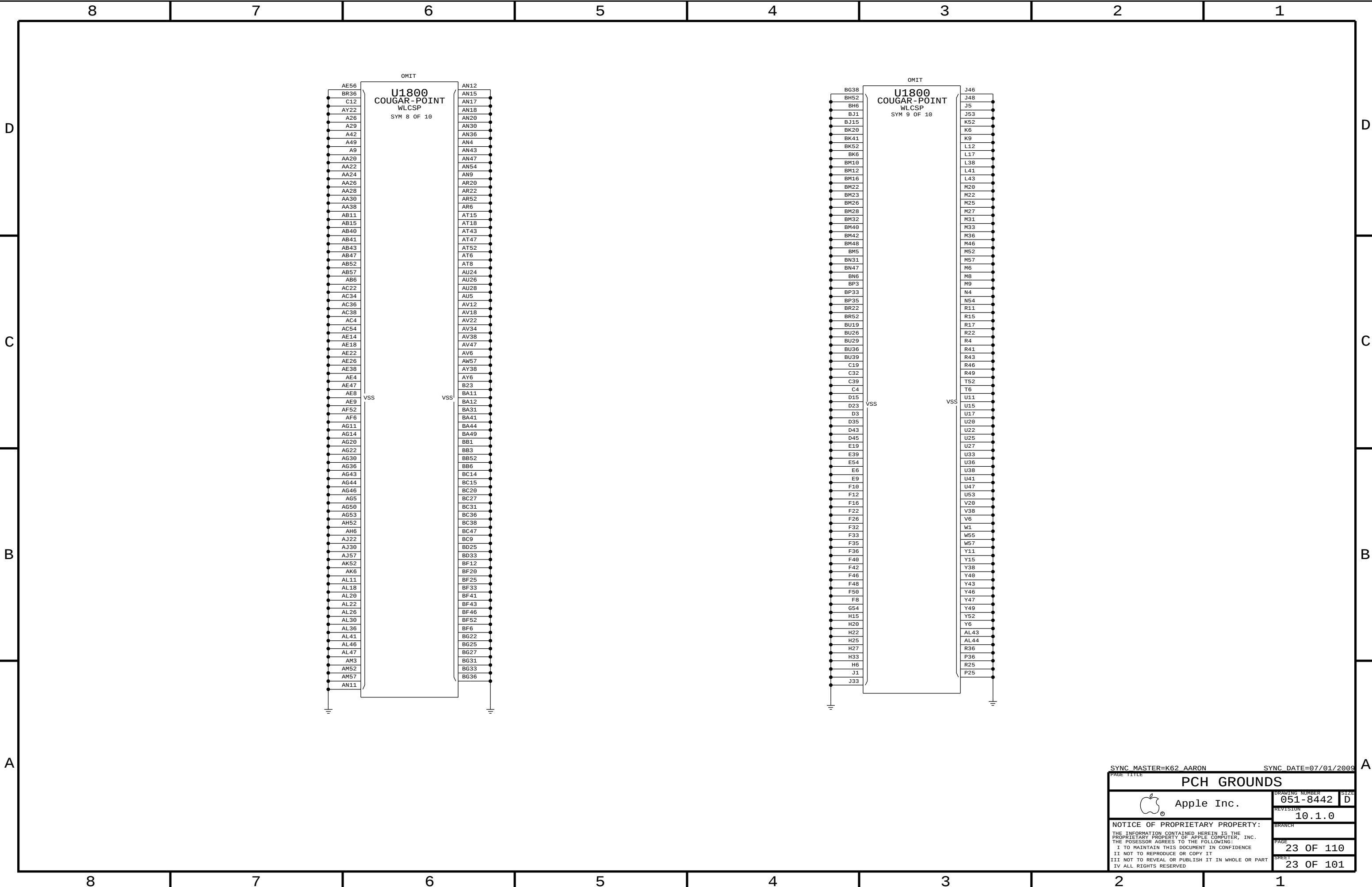








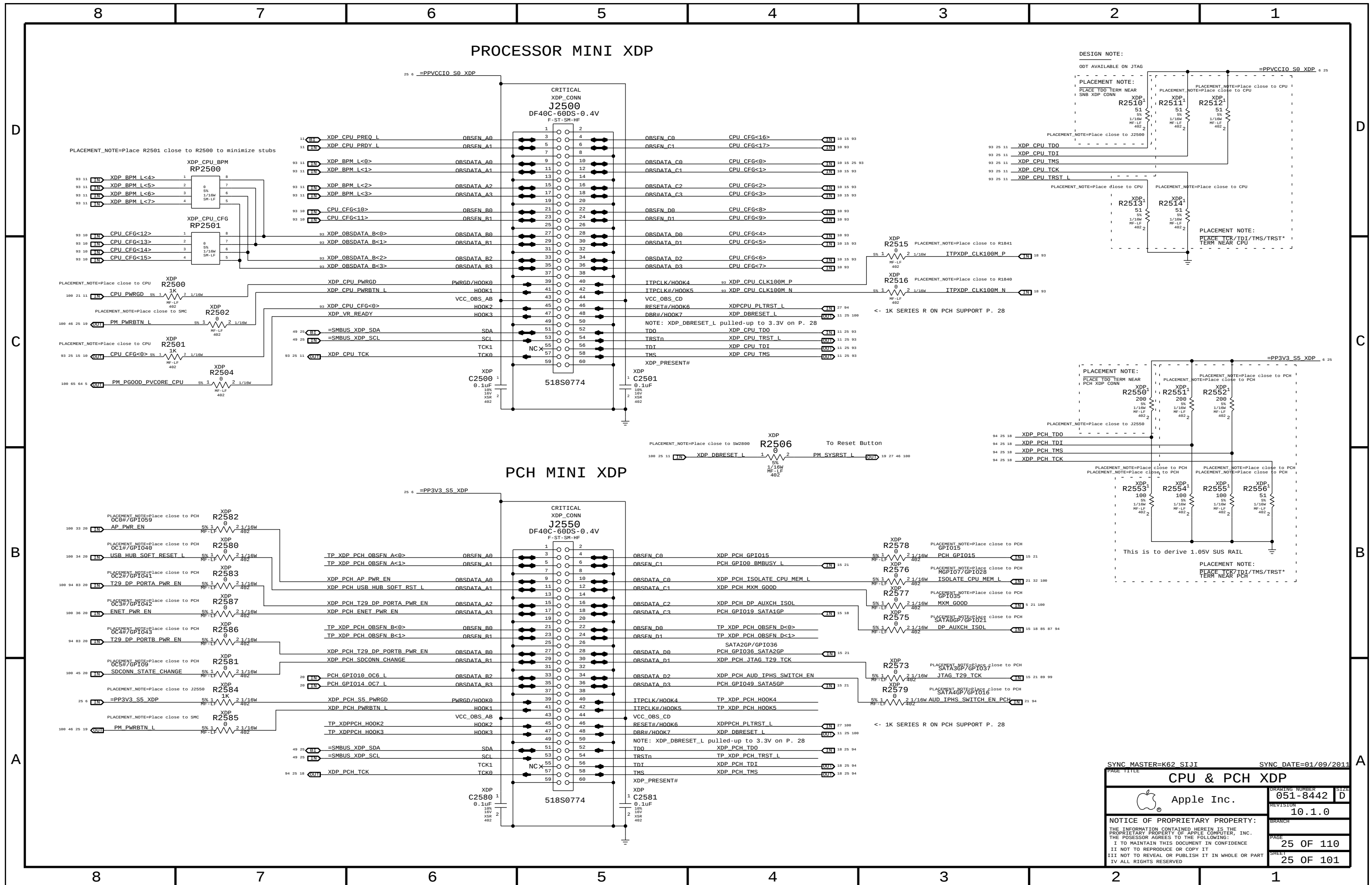




SYNC MASTER=K62 AARON

SYNC DATE=07/01/2009

PAGE TITLE		PCH GROUNDS	
 Apple Inc.		DRAWING NUMBER	051-8442
		REVISION	10.1.0
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		PAGE	23 OF 110
		SHEET	23 OF 101



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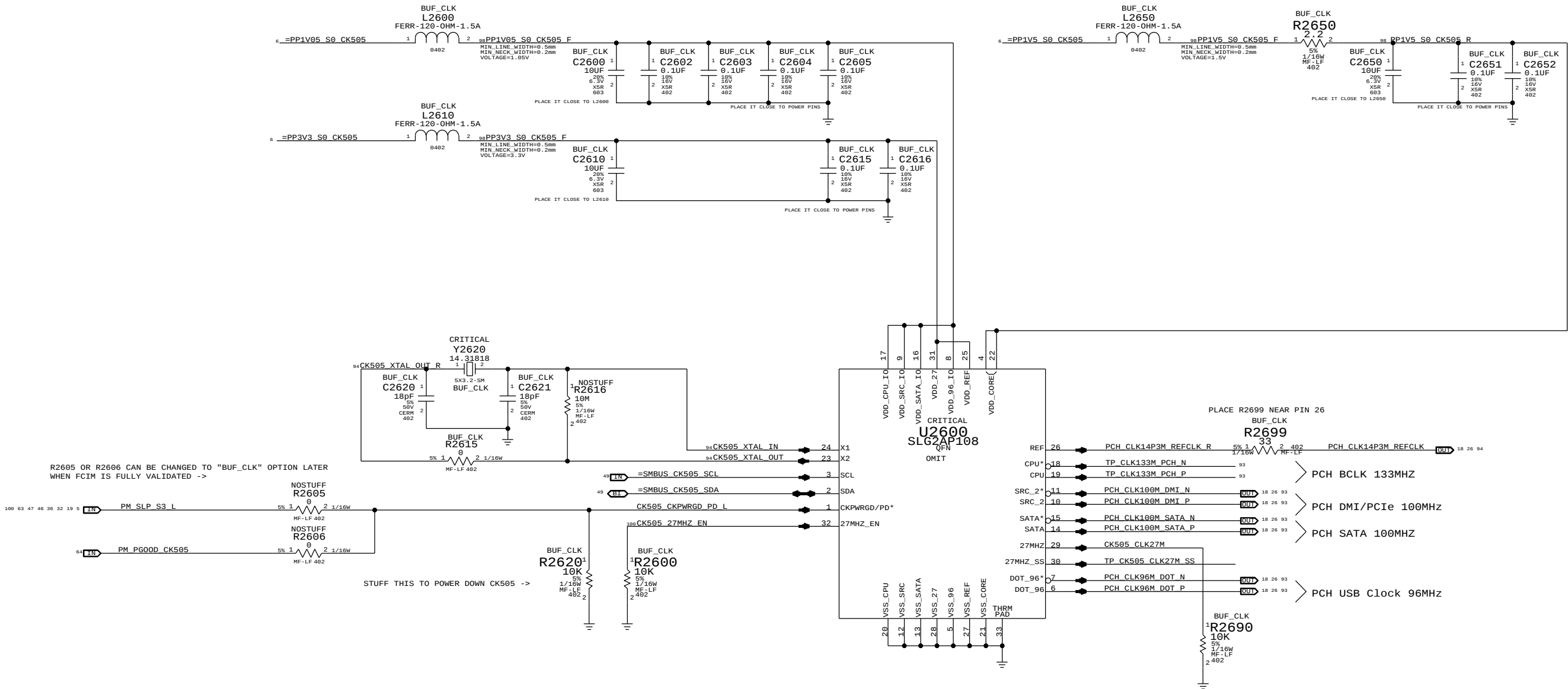
A

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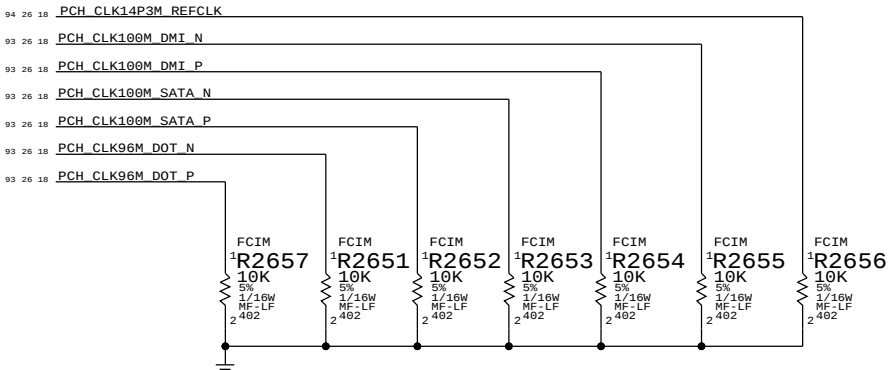
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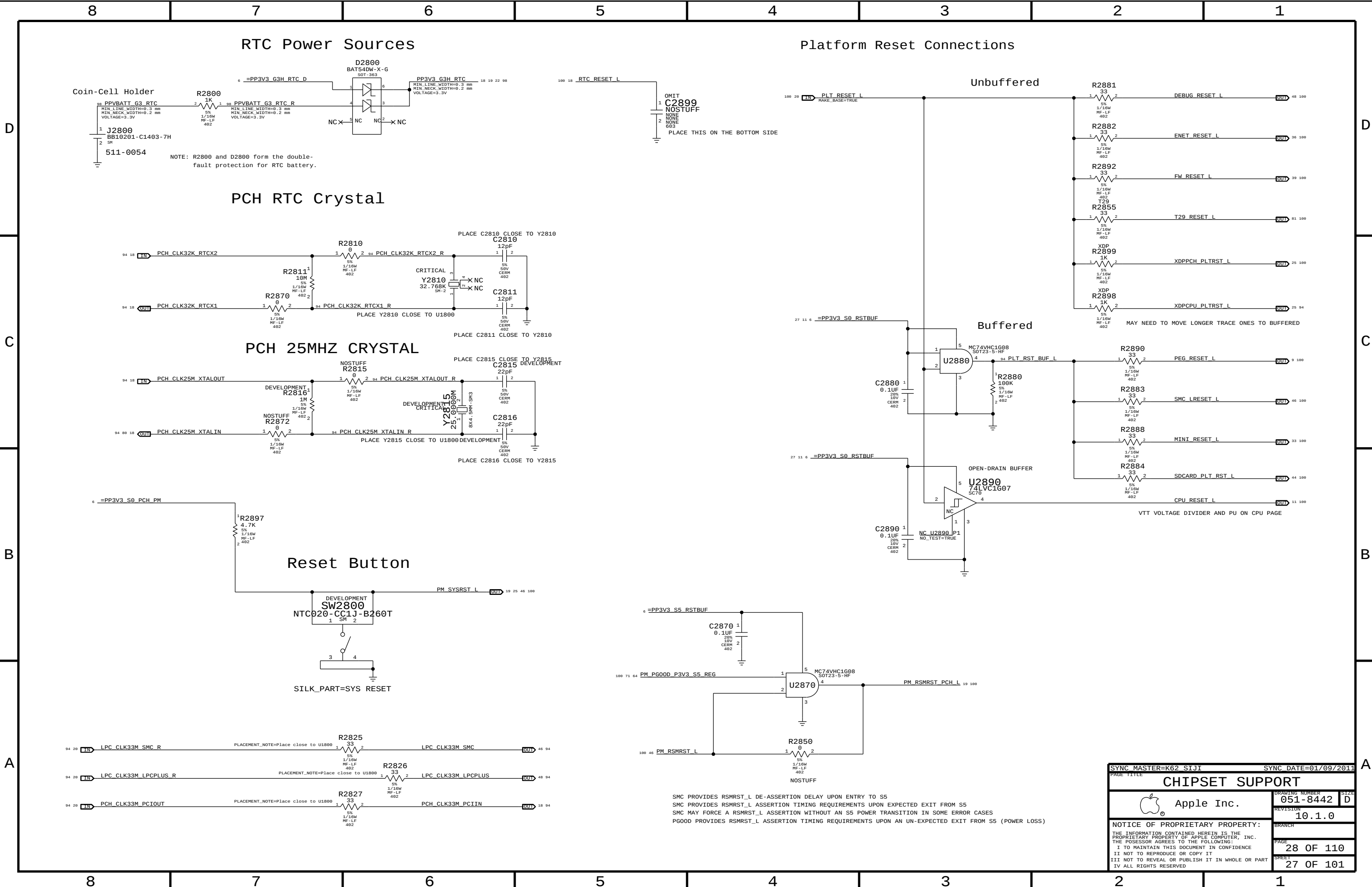
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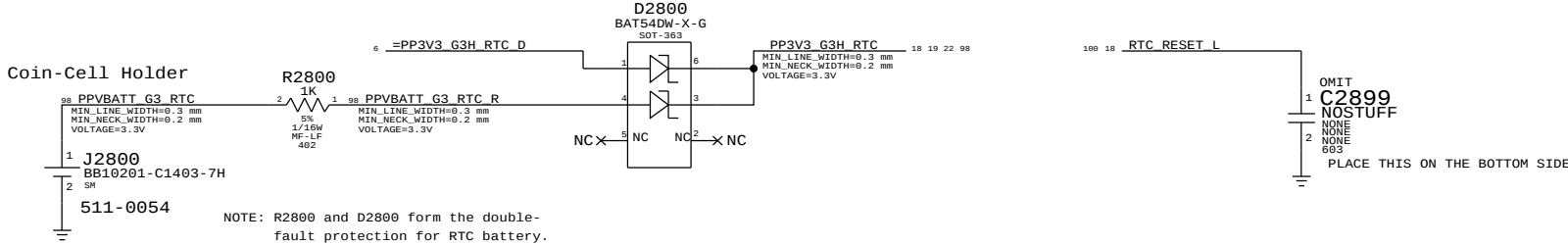
UNUSED clock terminations for FCIM MODE



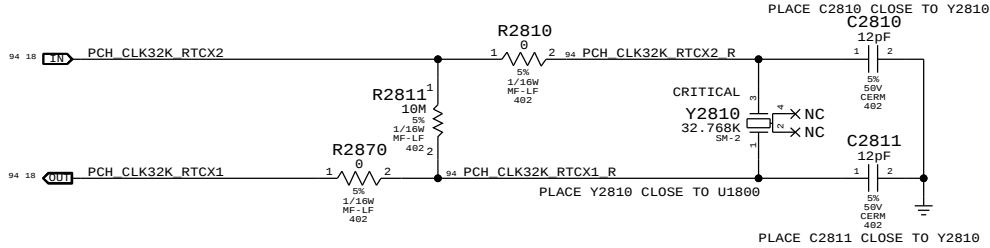
PAGE TITLE		SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
CLOCK (CK505)		DRAWING NUMBER		SIZE	
Apple Inc.		051-8442		D	
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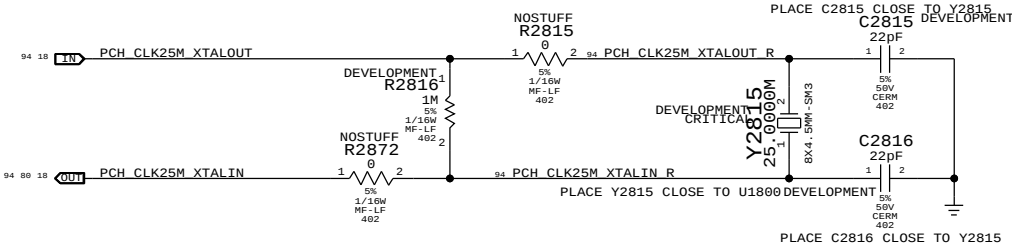
RTC Power Sources



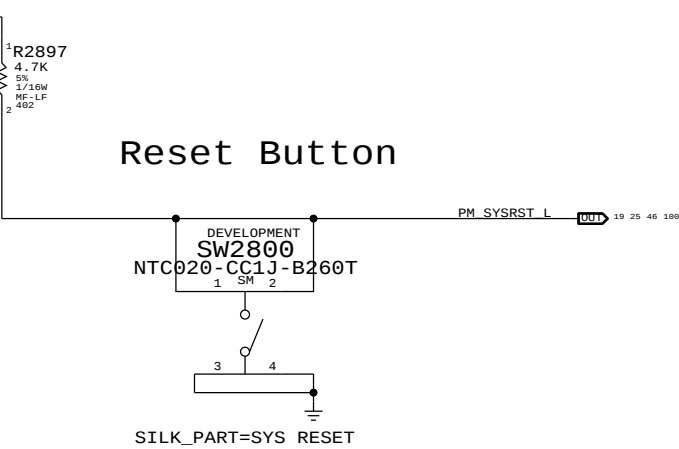
PCH RTC Crystal



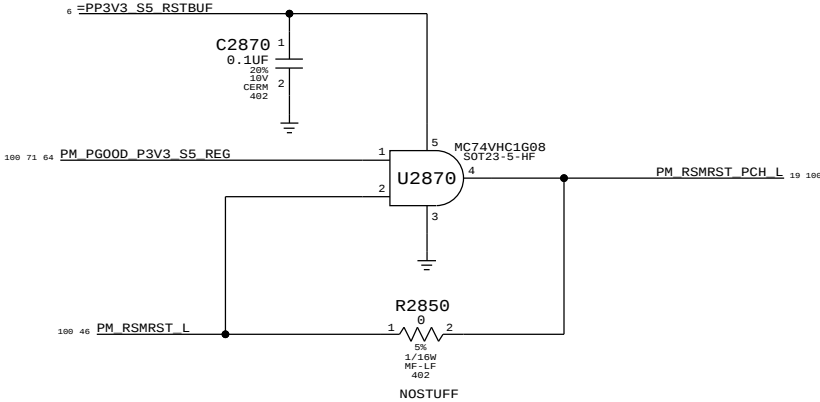
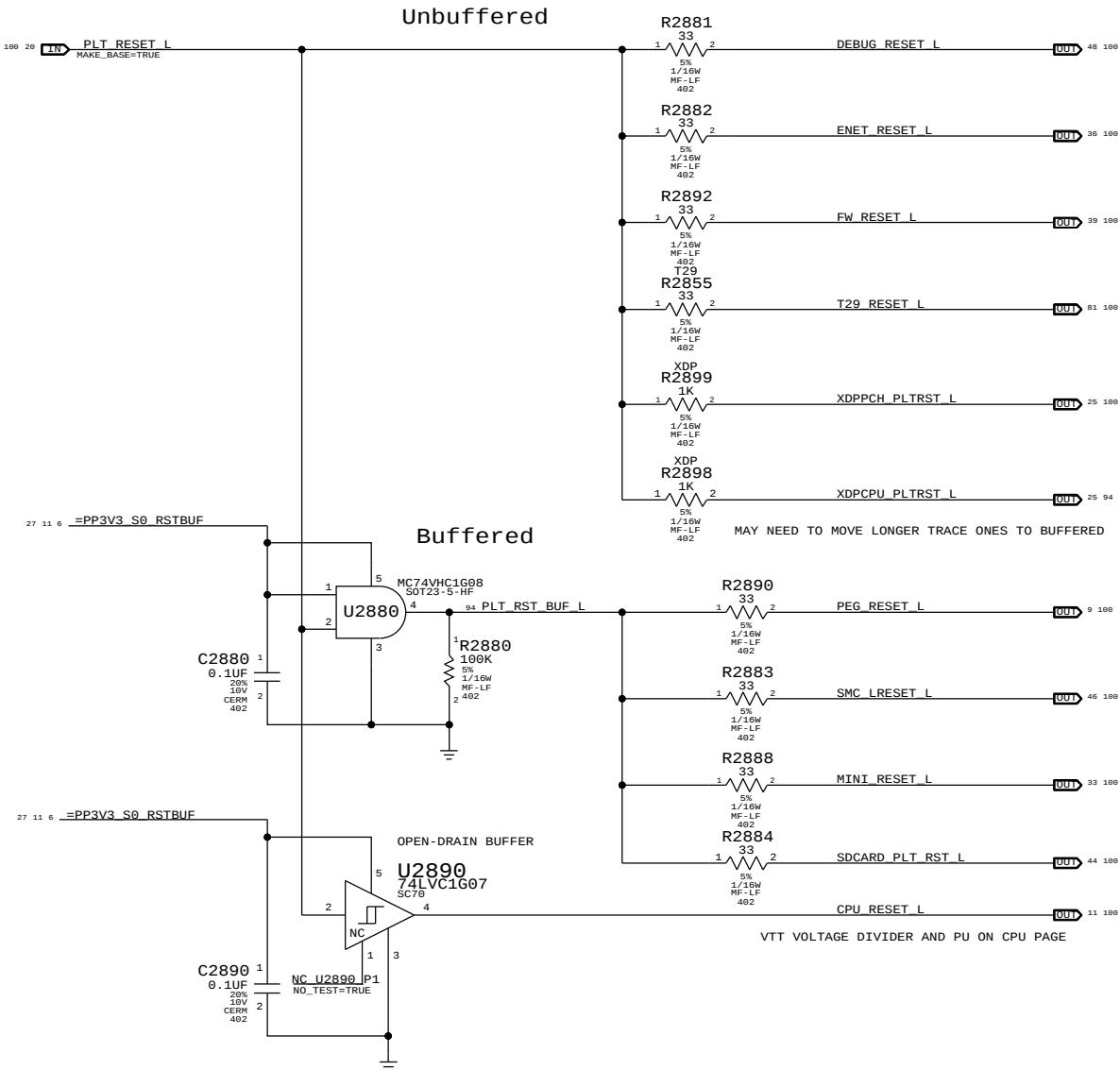
PCH 25MHZ CRYSTAL



Reset Button

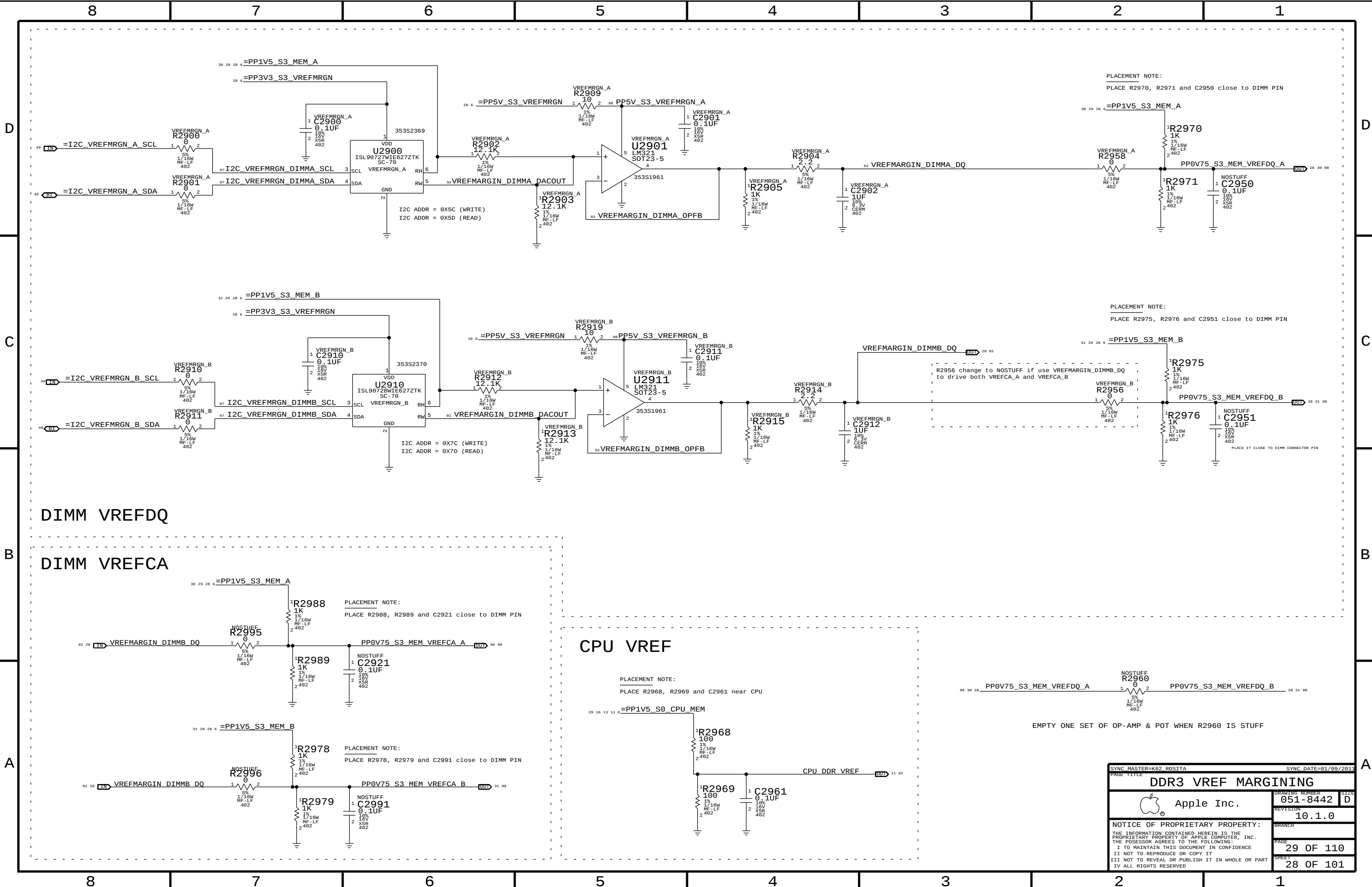


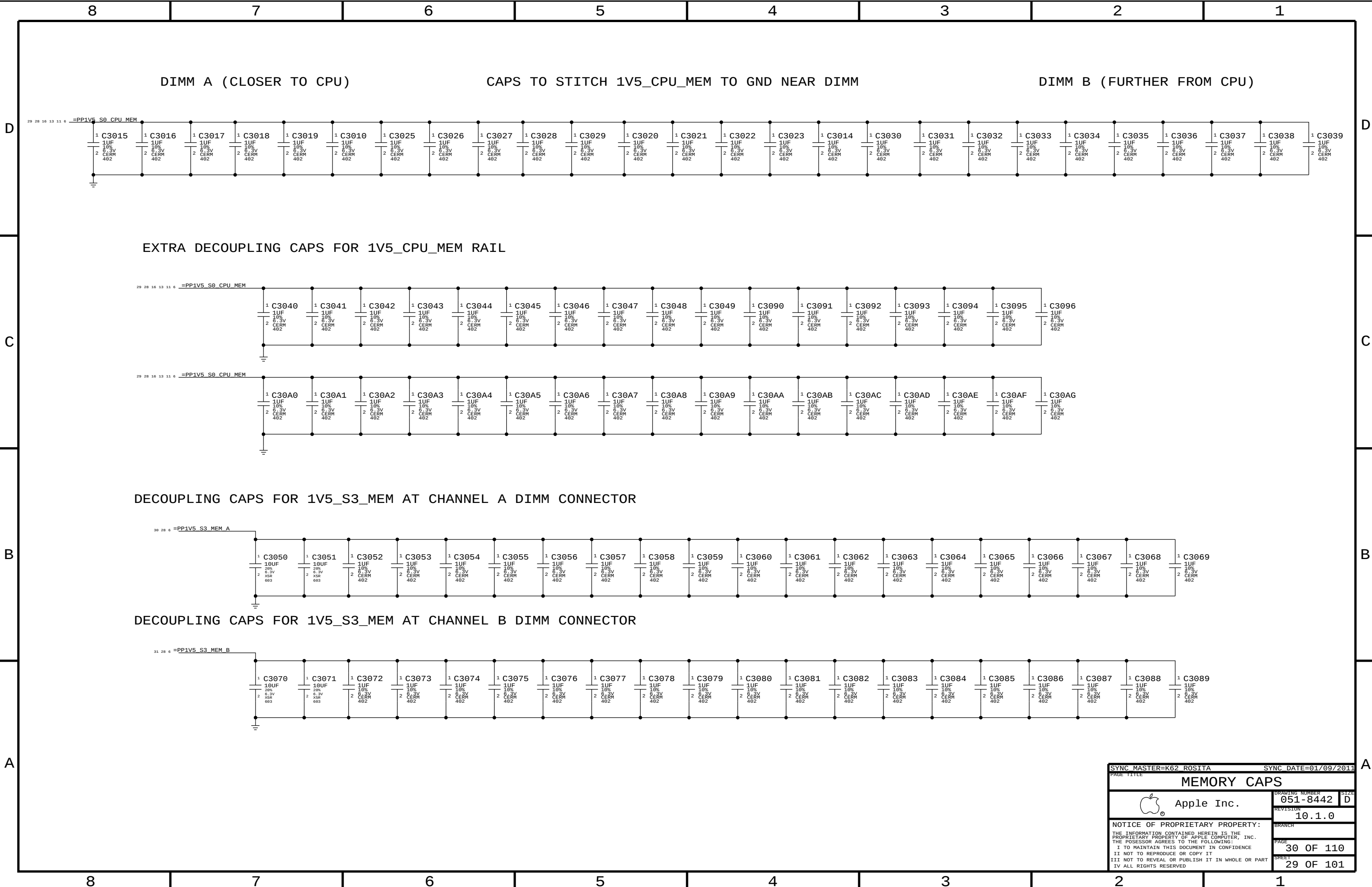
Platform Reset Connections



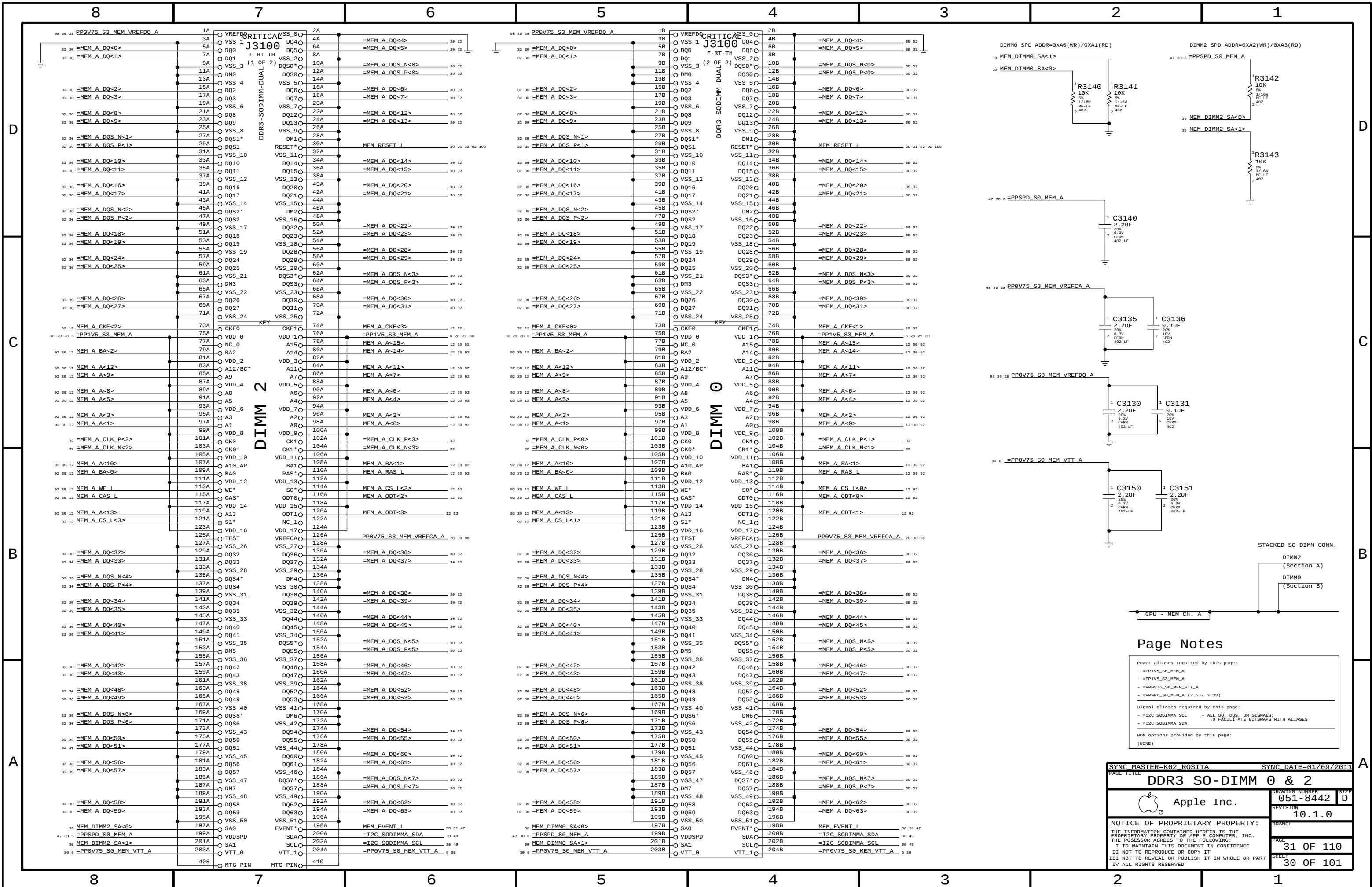
SMC PROVIDES RSMRST_L DE-ASSERTION DELAY UPON ENTRY TO S5
SMC PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON EXPECTED EXIT FROM S5
SMC MAY FORCE A RSMRST_L ASSERTION WITHOUT AN S5 POWER TRANSITION IN SOME ERROR CASES
PGOOD PROVIDES RSMRST_L ASSERTION TIMING REQUIREMENTS UPON AN UN-EXPECTED EXIT FROM S5 (POWER LOSS)

SYNC MASTER=K62 SIJI		SYNC DATE=01/09/2011	
PAGE TITLE		CHIPSET SUPPORT	
 Apple Inc.		DRAWING NUMBER	051-8442
		REVISION	10.1.0
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SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
PAGE TITLE		MEMORY CAPS	
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		REVISION	10.1.0
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		PAGE	30 OF 110
		SHEET	29 OF 101



Page Notes

Power aliases required by this page:

- #PP1V5_S0_MEM_A
- #PP1V5_S3_MEM_A
- #PP0V75_S0_MEM_VTT_A
- #PPSPD_S0_MEM_A (2.5 - 3.3V)

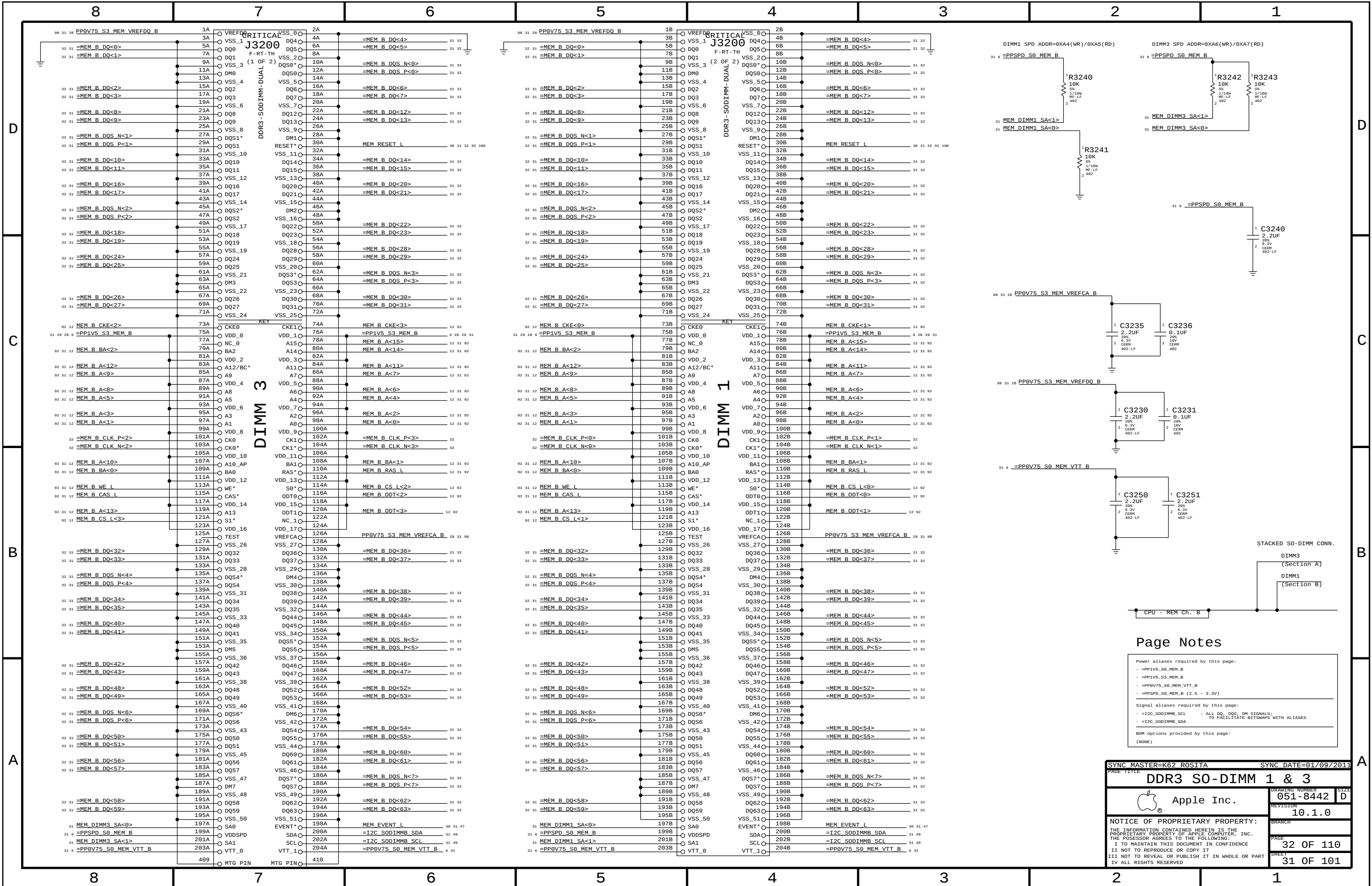
Signal aliases required by this page:

- #I2C_SODIMMA_SCL - ALL DQ, DQS, DM SIGNALS; TO FACILITATE BITMAPS WITH ALIASES
- #I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
PAGE TITLE			
DDR3 SO-DIMM 0 & 2		DRAWING NUMBER	
Apple Inc.		051-8442	
REVISION		SIZE	
10.1.0		D	
BRANCH		PAGE	
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_S0DIMMB_SCL - ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITMAPS WITH ALIASES
- =I2C_S0DIMMB_SDA

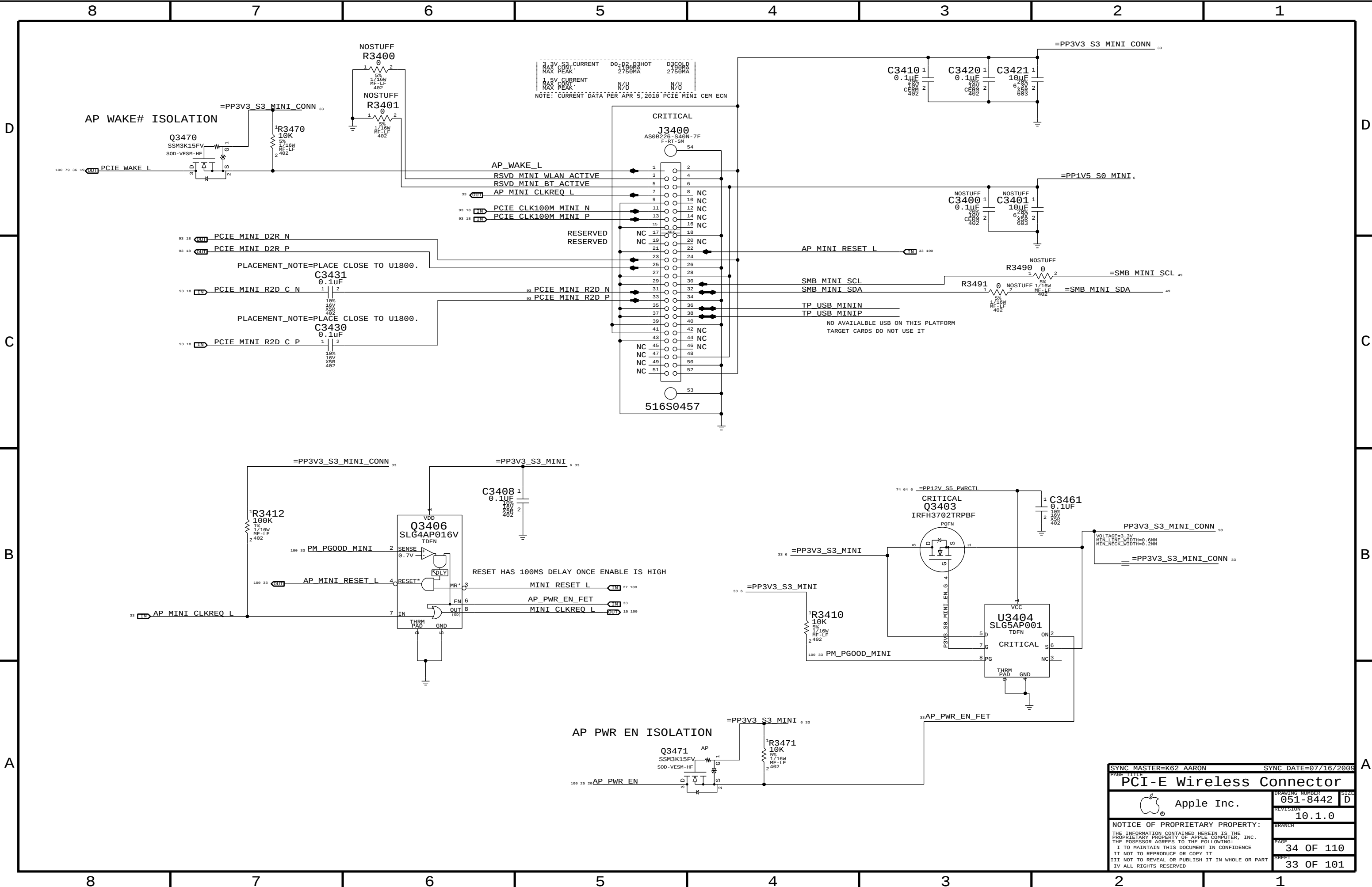
BOM options provided by this page:

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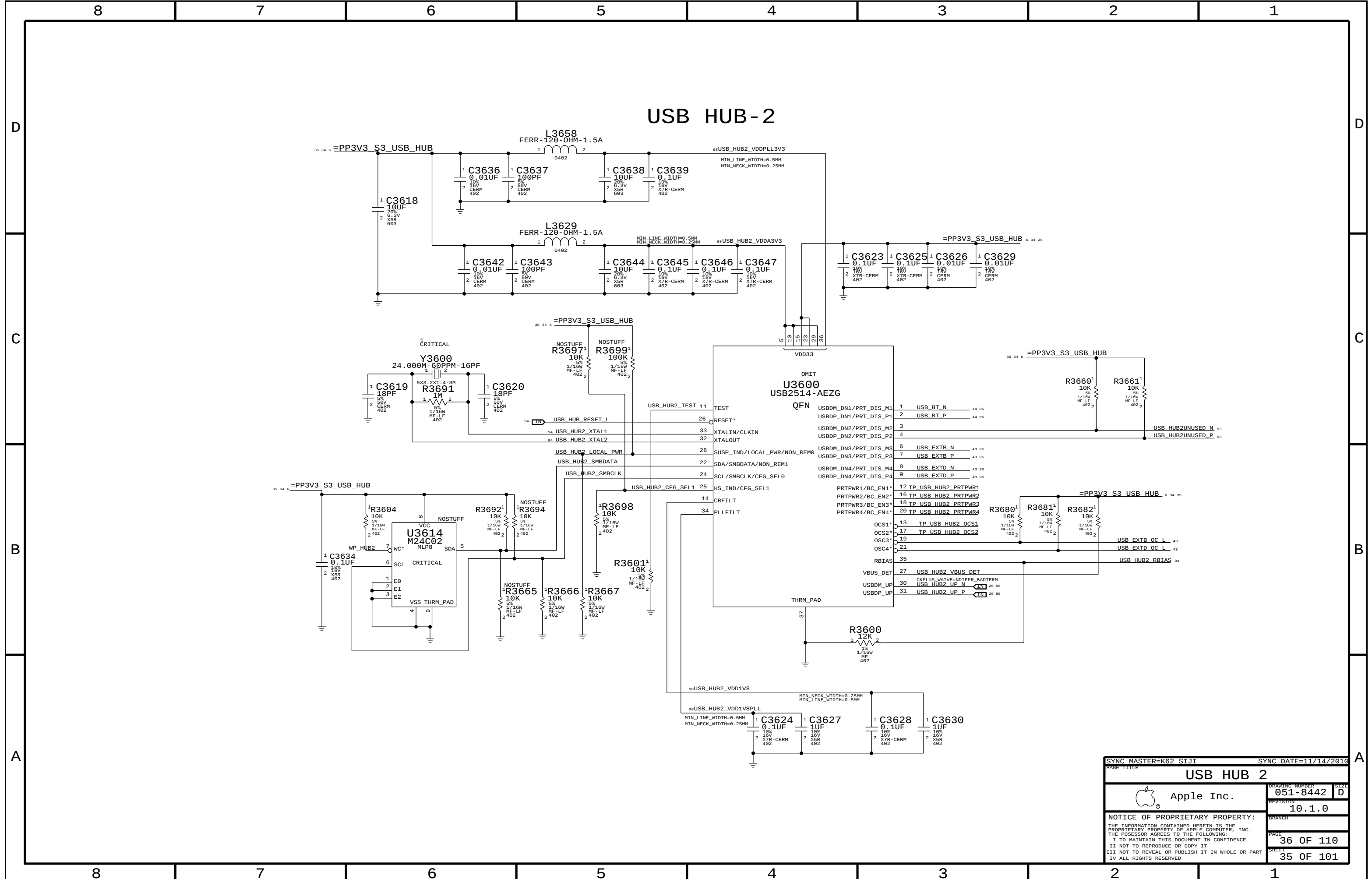
SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
PAGE TITLE		SIZE	
DDR3 SO-DIMM 1 & 3		051-8442	
Apple Inc.		REVISION	
		10.1.0	
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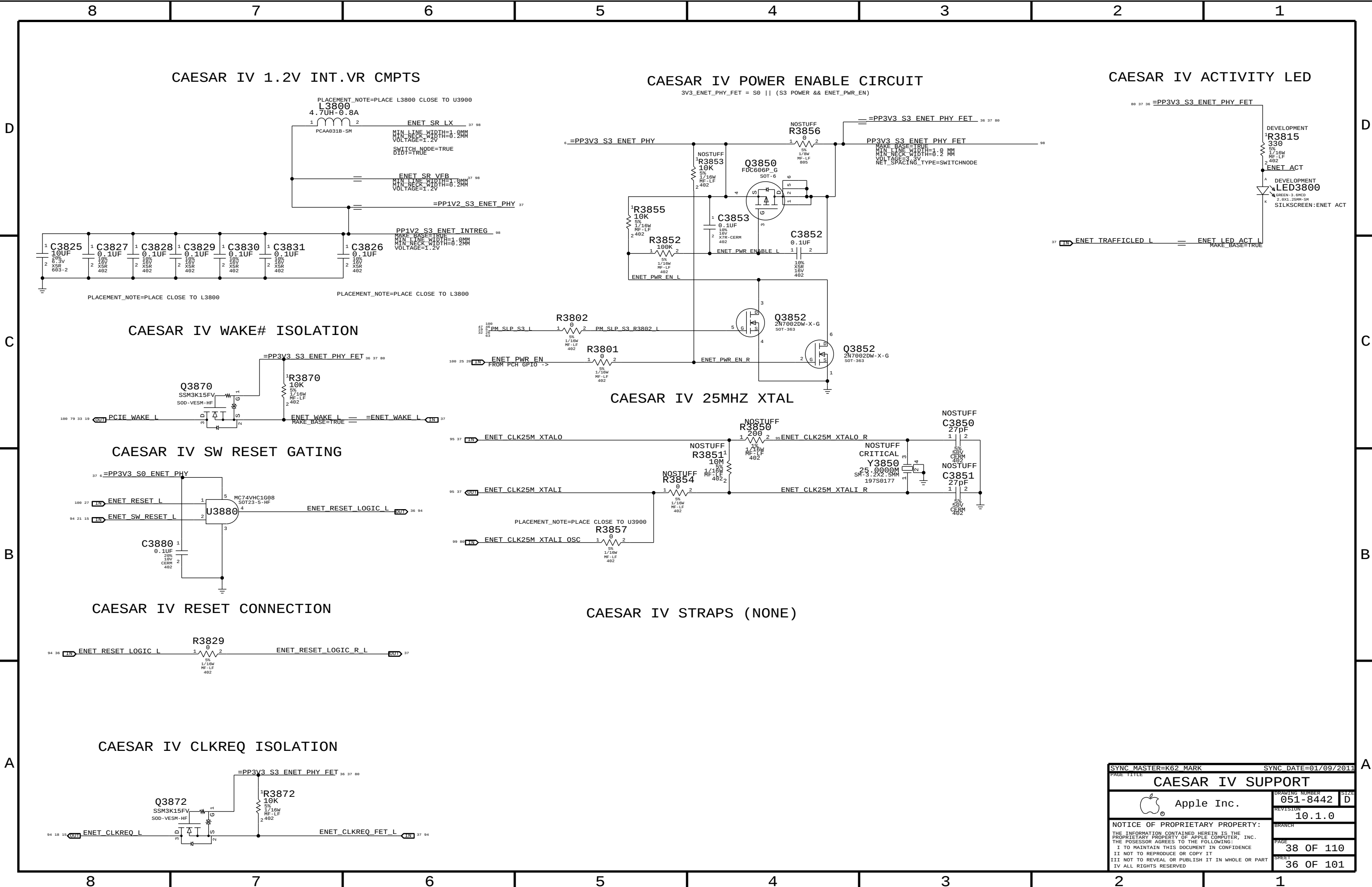
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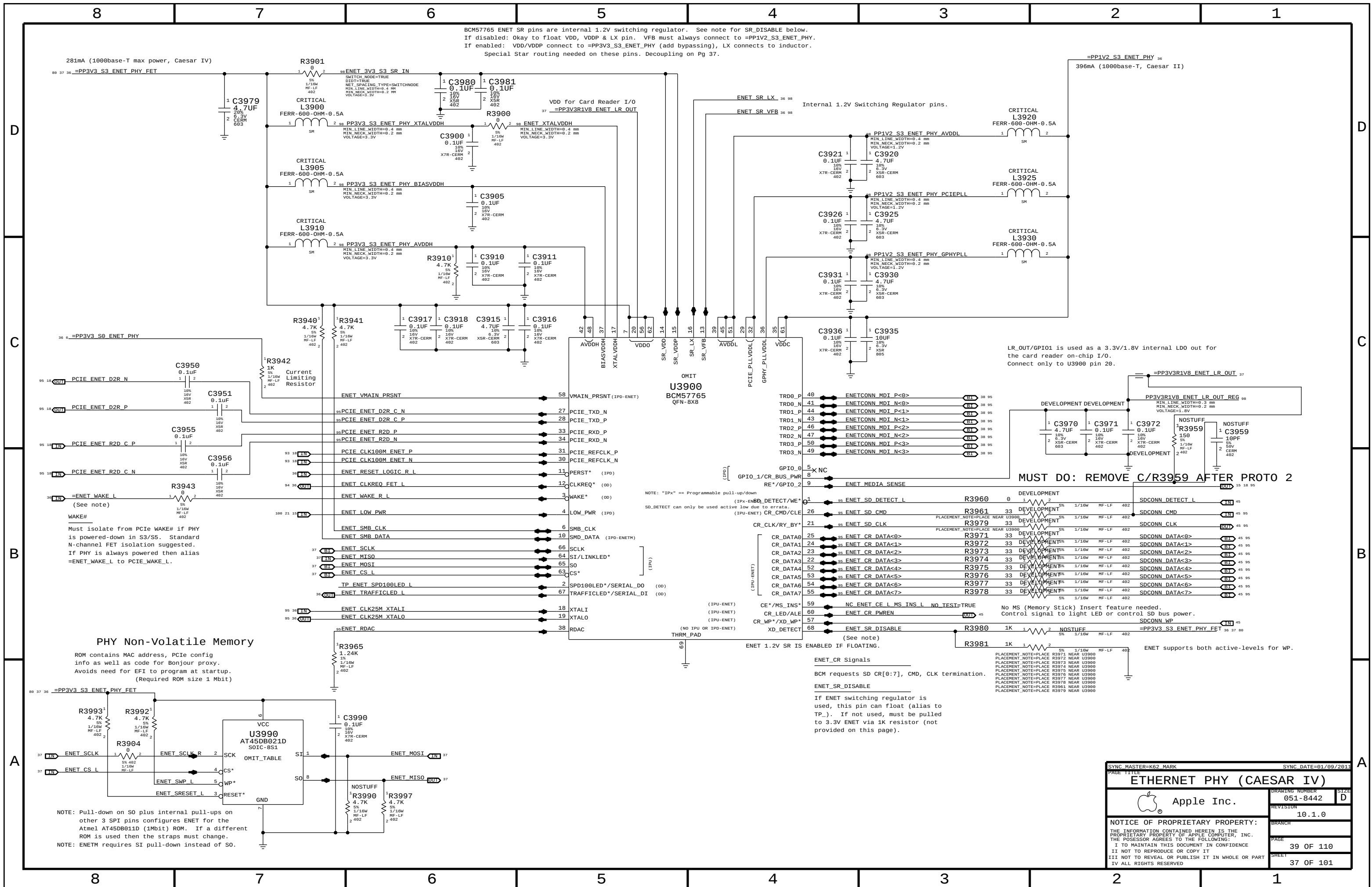
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PAGE TITLE			
PCI-E Wireless Connector			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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		BRANCH	
		PAGE	34 OF 110
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SYNC MASTER=K62 SIJI		SYNC DATE=11/14/2016	
PAGE TITLE			
USB HUB 2			
 Apple Inc.	DRAWING NUMBER		SIZE
	051-8442		D
		REVISION	
		10.1.0	
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SYNC MASTER=K62 MARK		SYNC DATE=01/09/2011	
PAGE TITLE			
CAESAR IV SUPPORT			
 Apple Inc.	DRAWING NUMBER	051-8442	SIZE D
	REVISION	10.1.0	
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PAGE		38 OF 110	
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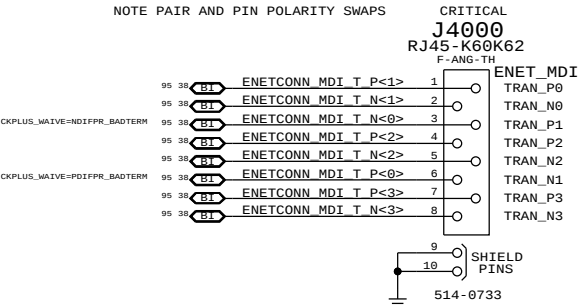
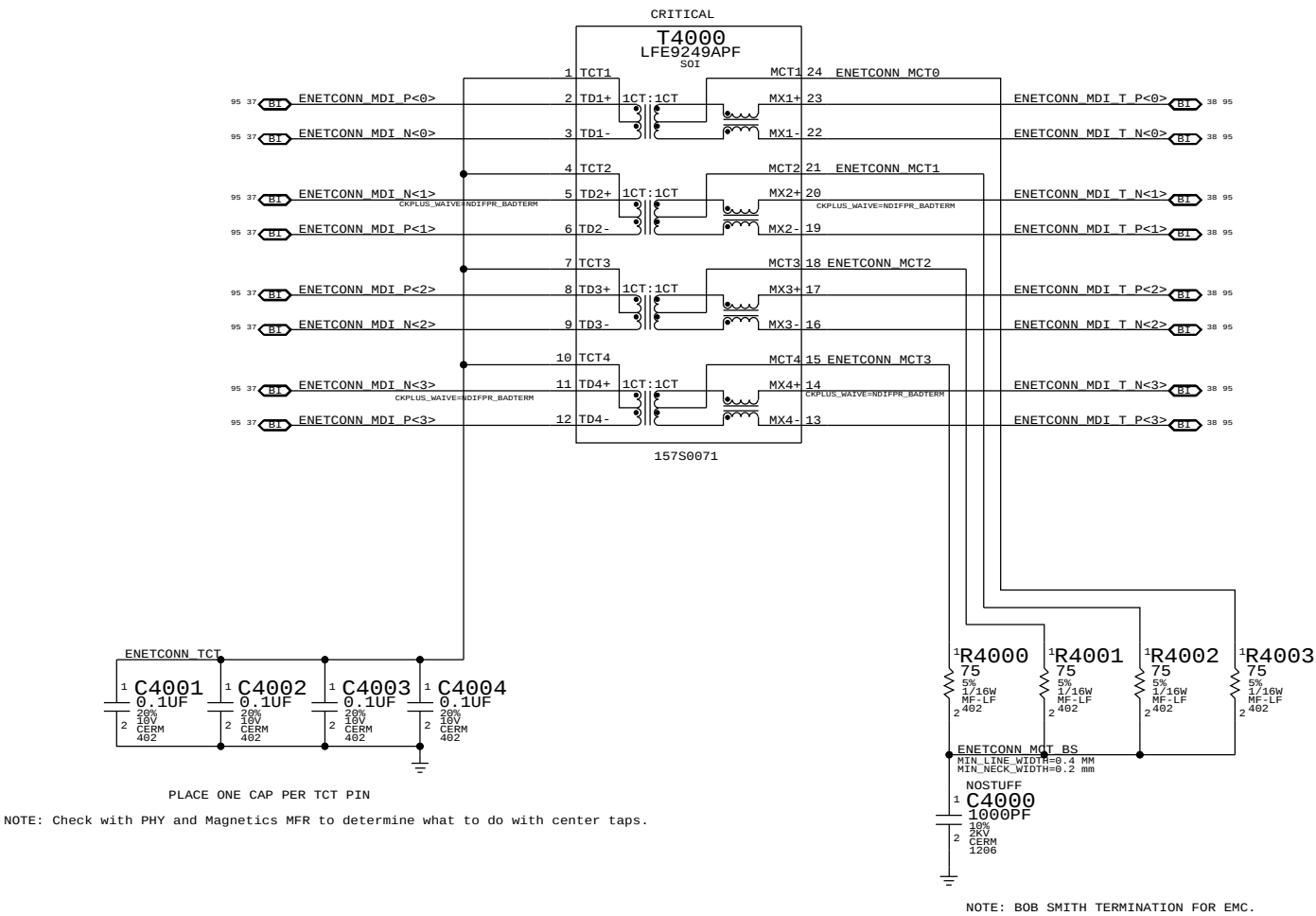
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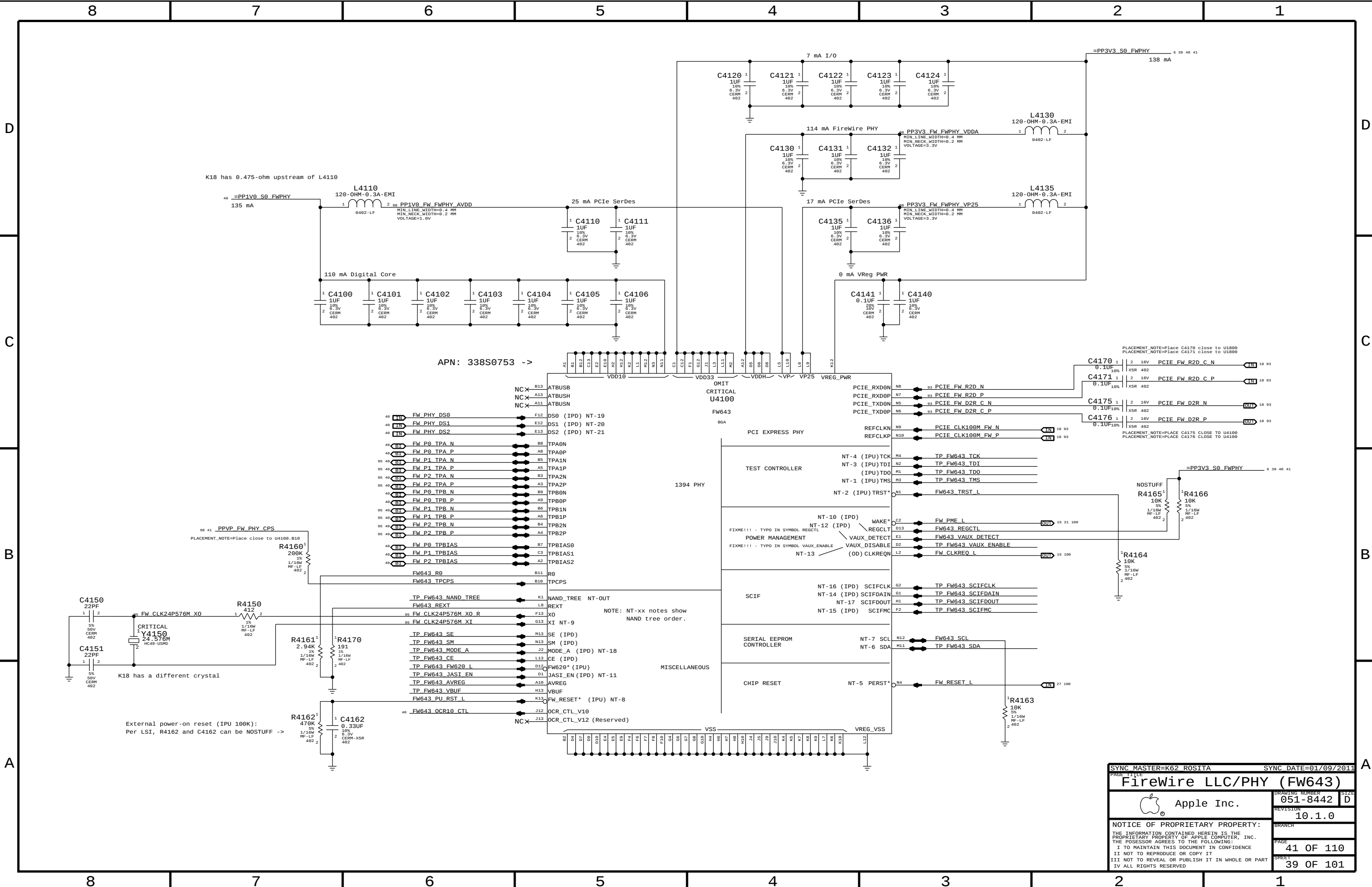
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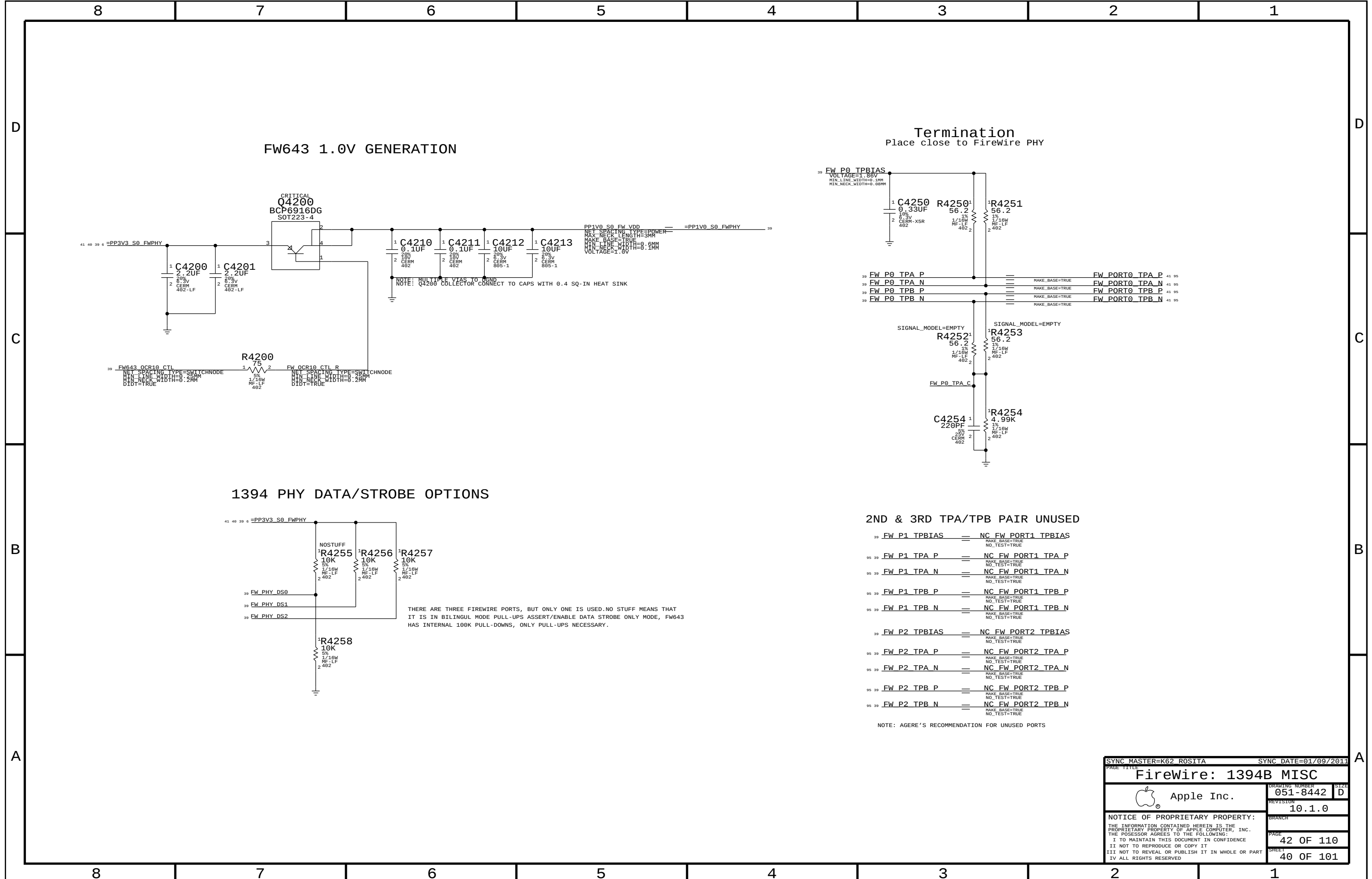
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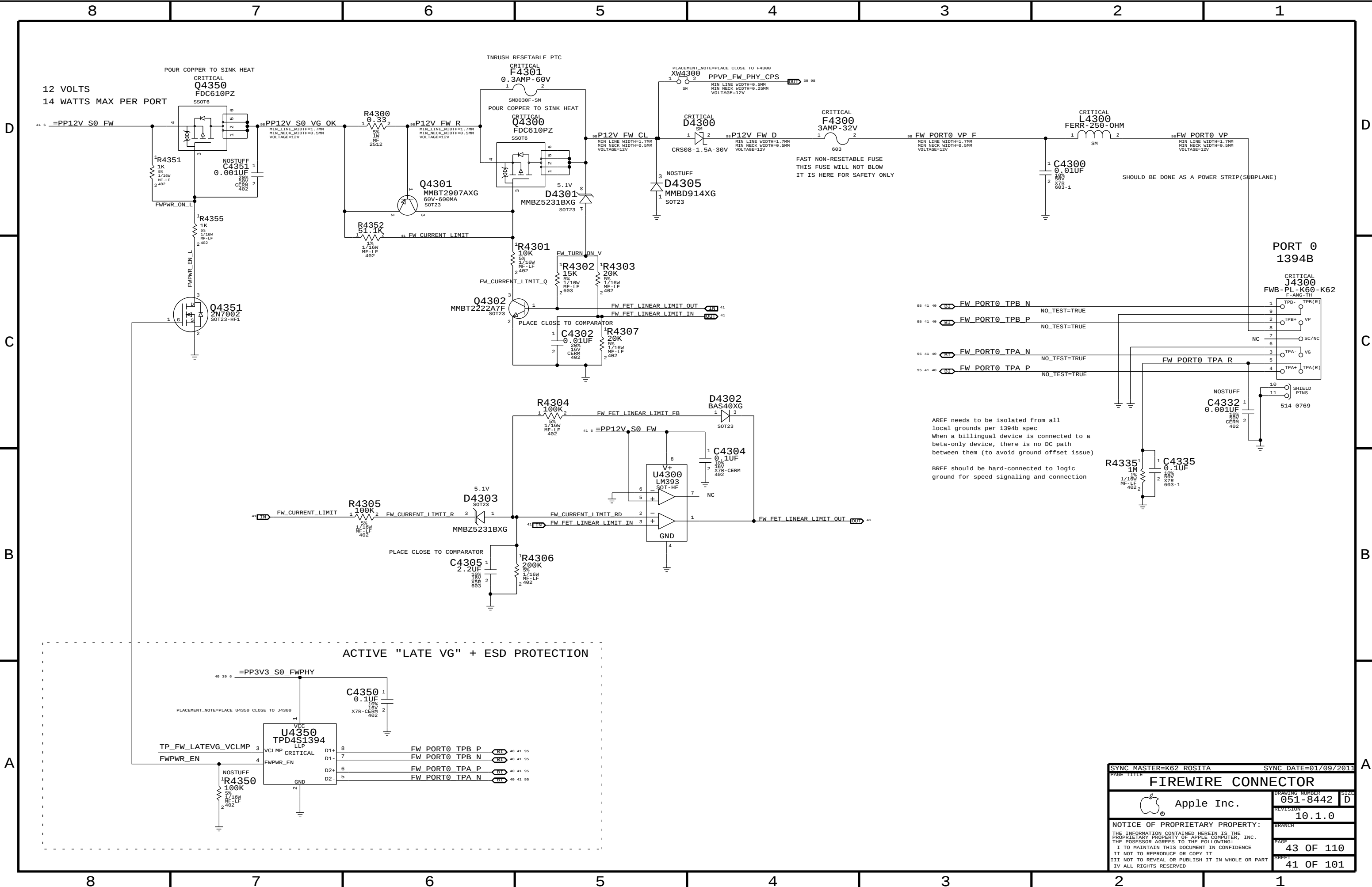
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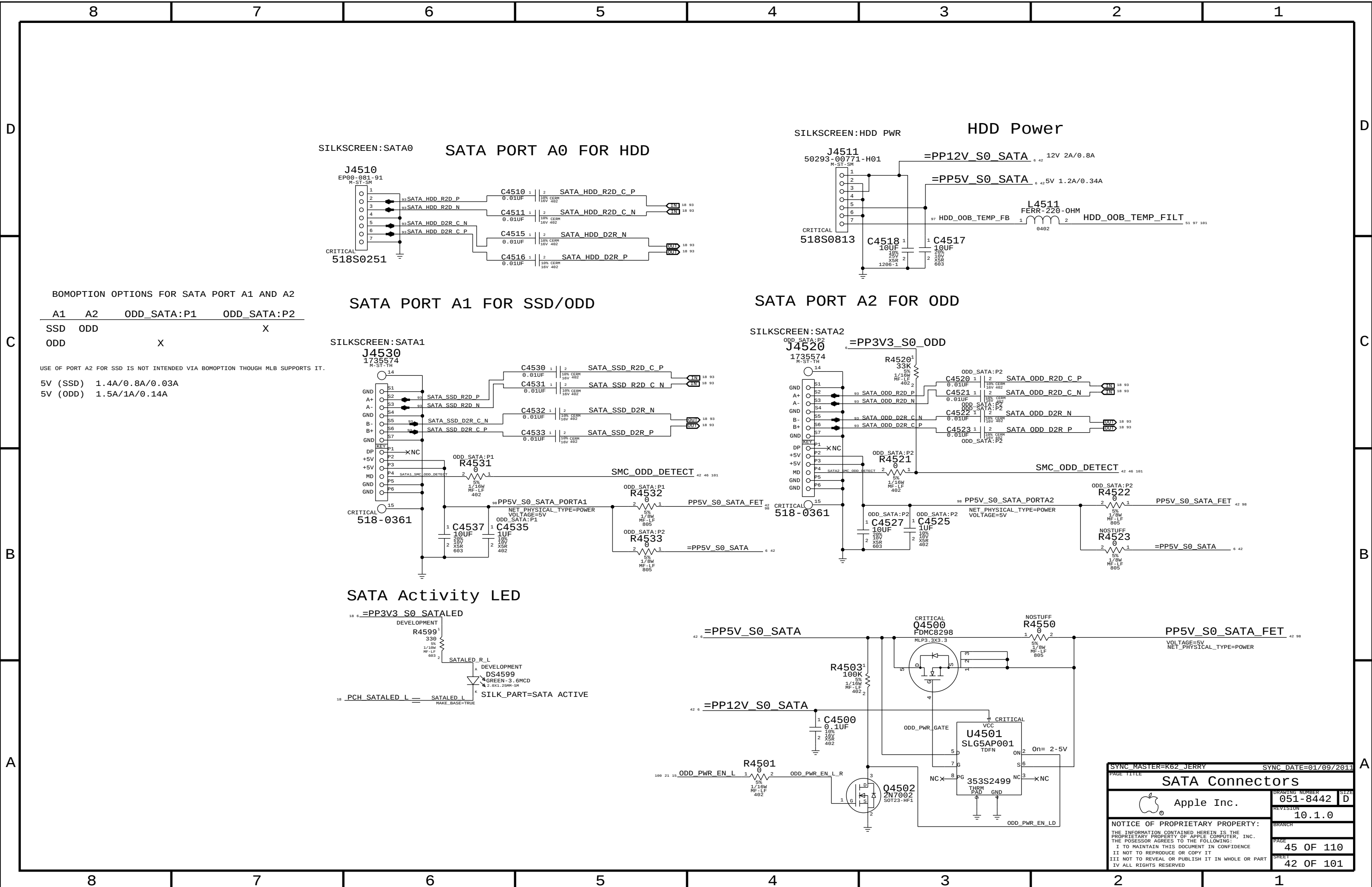
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PAGE TITLE		Ethernet Connector	
Apple Inc.		DRAWING NUMBER	051-8442
		REVISION	10.1.0
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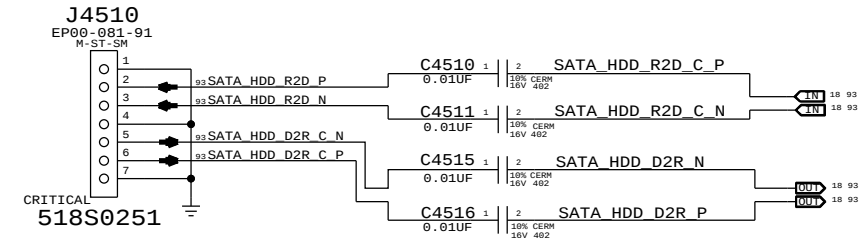


SYNC MASTER=K62 ROSITA		SYNC DATE=01/09/2011	
PAGE TITLE		FIREWIRE CONNECTOR	
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		REVISION	10.1.0
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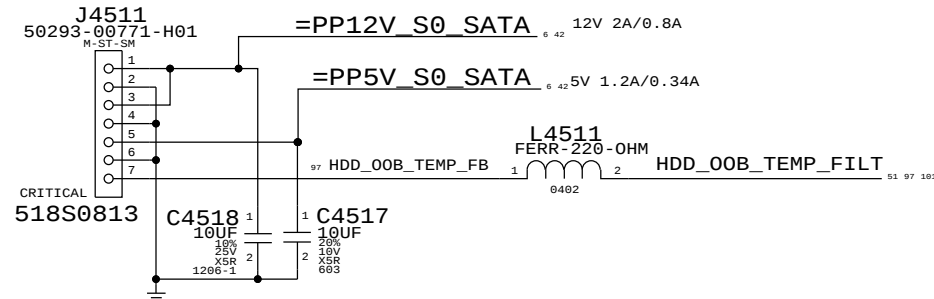
SILKSCREEN:SATA0

SATA PORT A0 FOR HDD



SILKSCREEN:HDD PWR

HDD Power

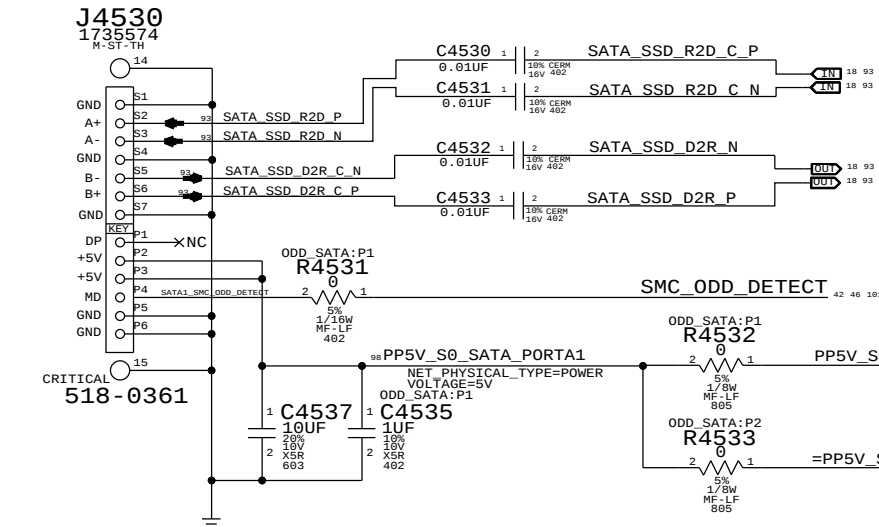


BOMOPTION OPTIONS FOR SATA PORT A1 AND A2

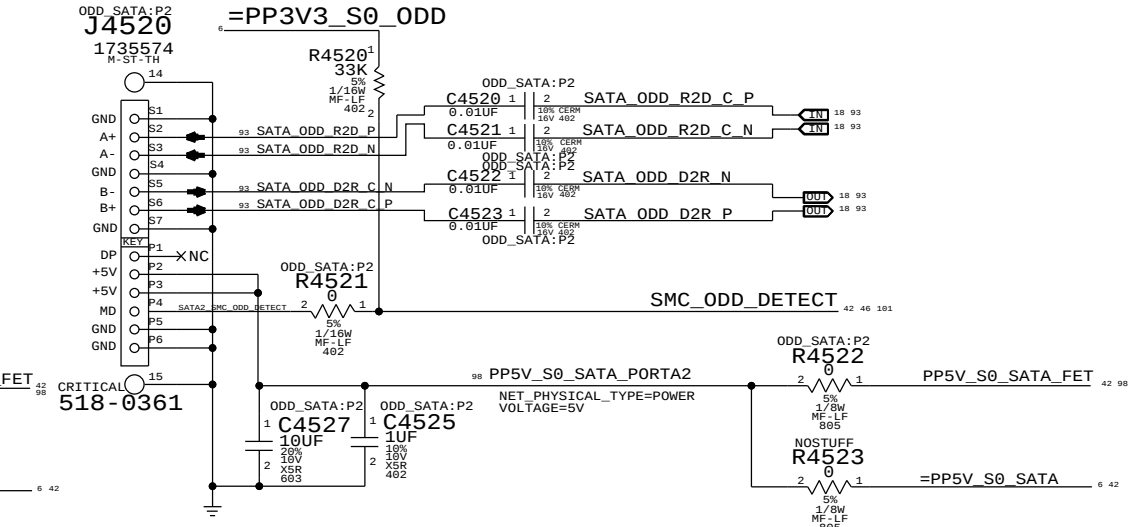
A1	A2	ODD_SATA:P1	ODD_SATA:P2
SSD	ODD		X
ODD		X	

SATA PORT A1 FOR SSD/ODD

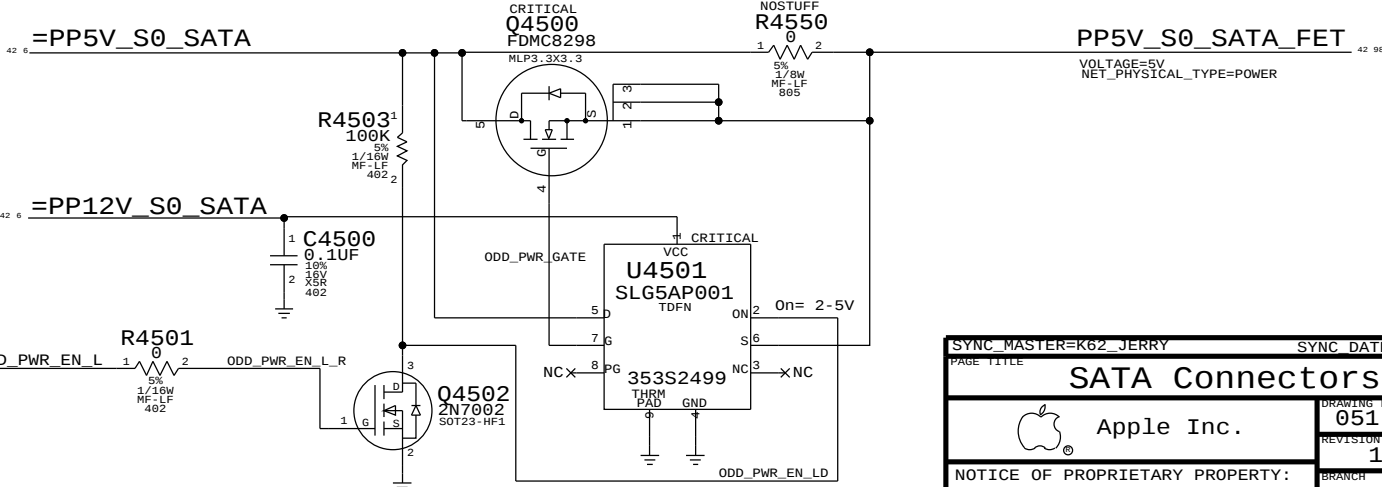
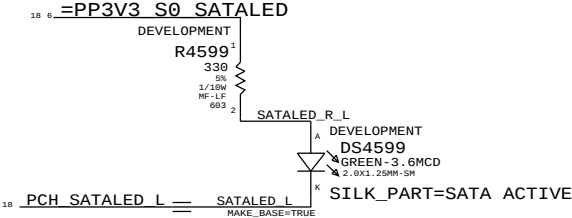
SILKSCREEN:SATA1



SILKSCREEN:SATA2



SATA Activity LED



SYNC MASTER=K62_JERRY		SYNC DATE=01/09/2011	
PAGE TITLE		SATA Connectors	
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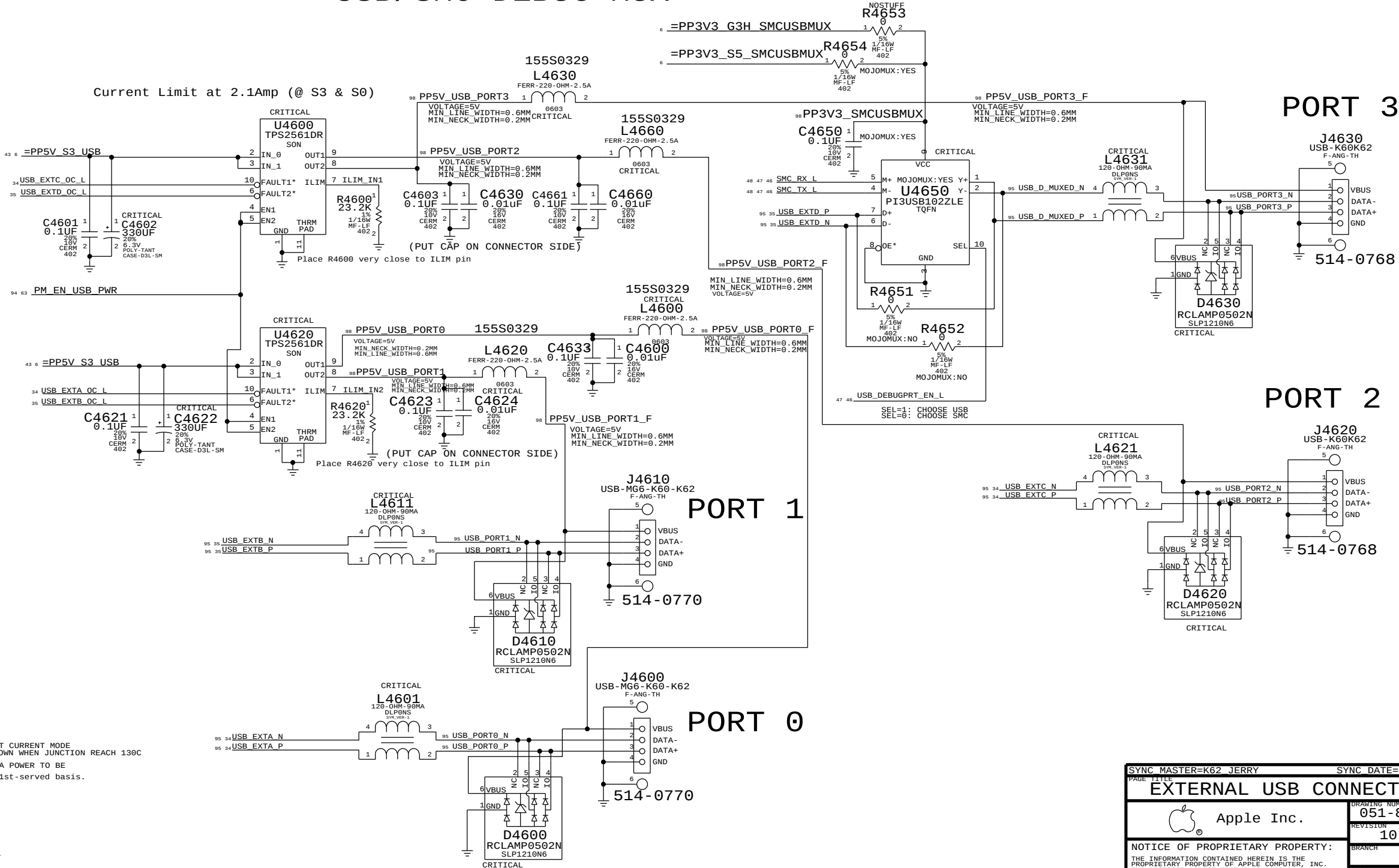
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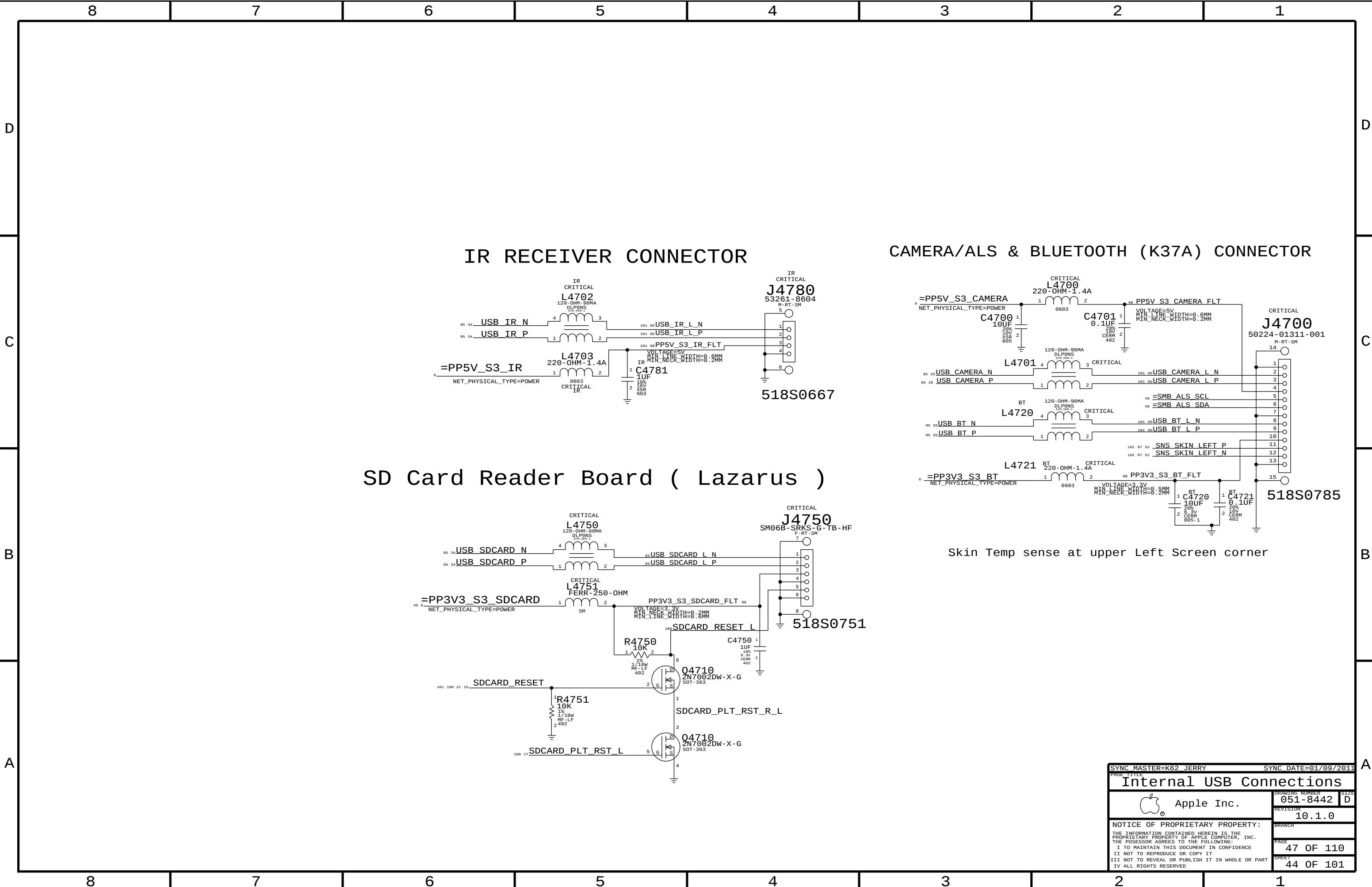
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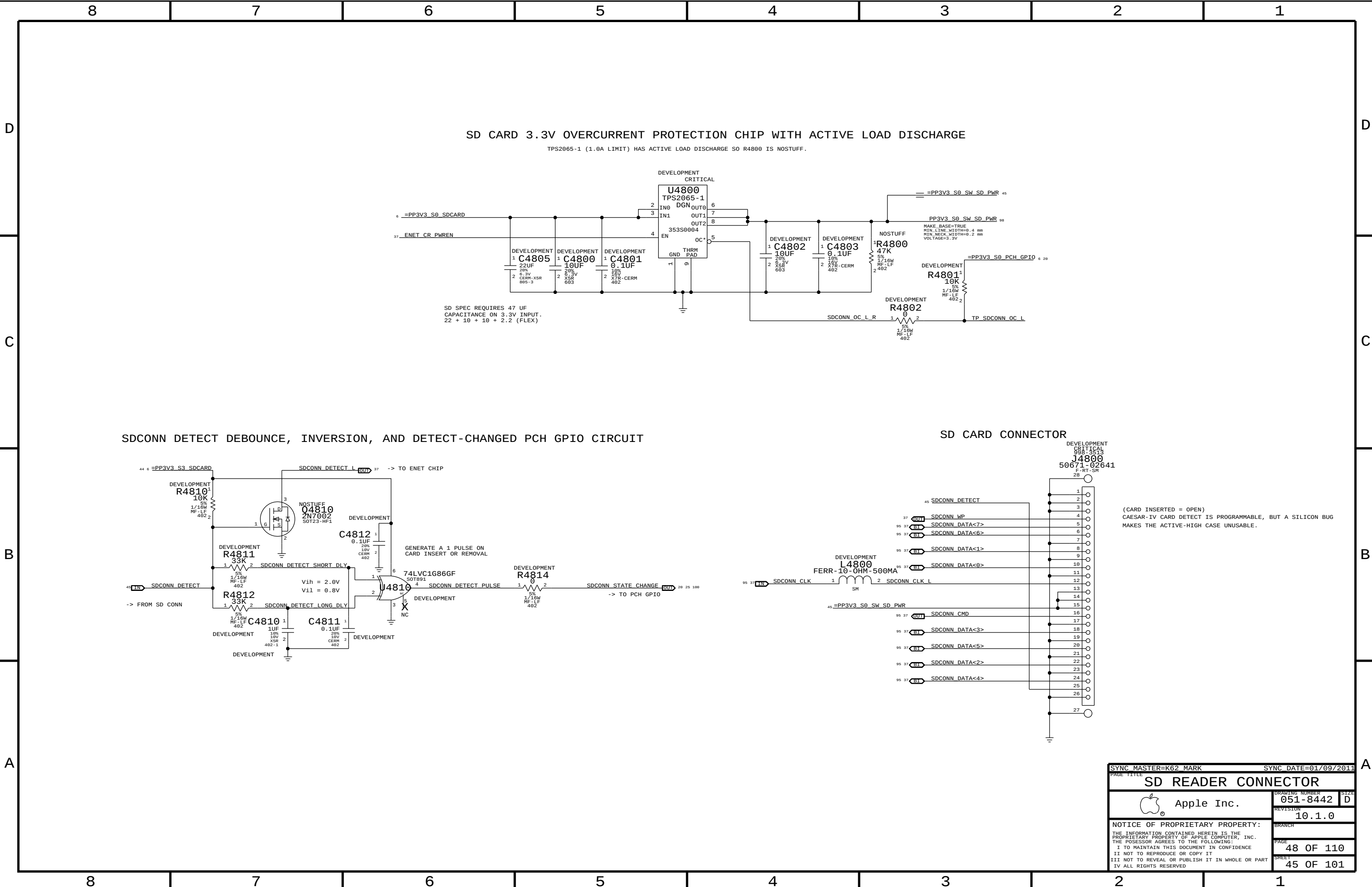
USB/SMC DEBUG MUX

ADDED AT EVT & SWITCH TO S5 RAIL



SYNC MASTER=K62 JERRY		SYNC DATE=01/09/2011	
PAGE TITLE			
EXTERNAL USB CONNECTORS			
 Apple Inc.		DRAWING NUMBER	051-8442
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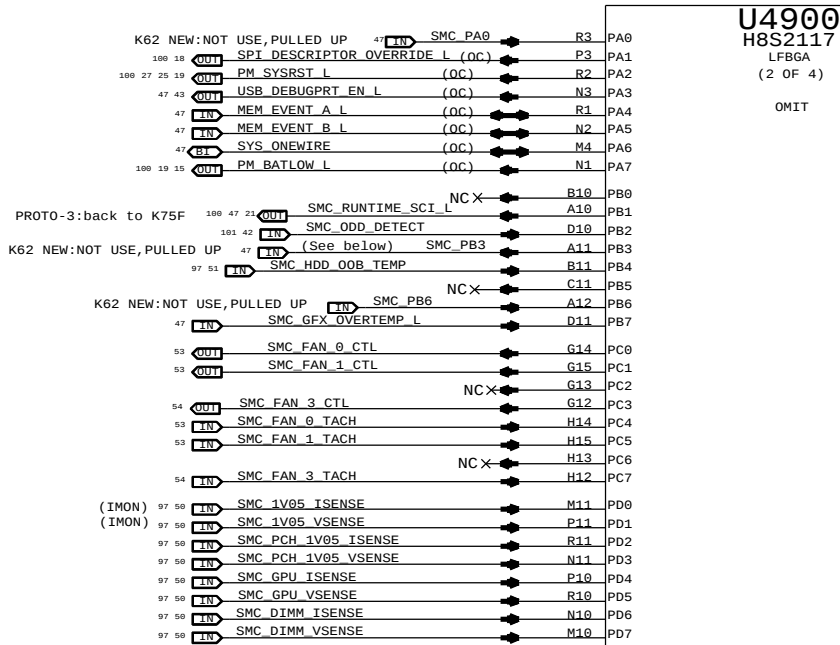
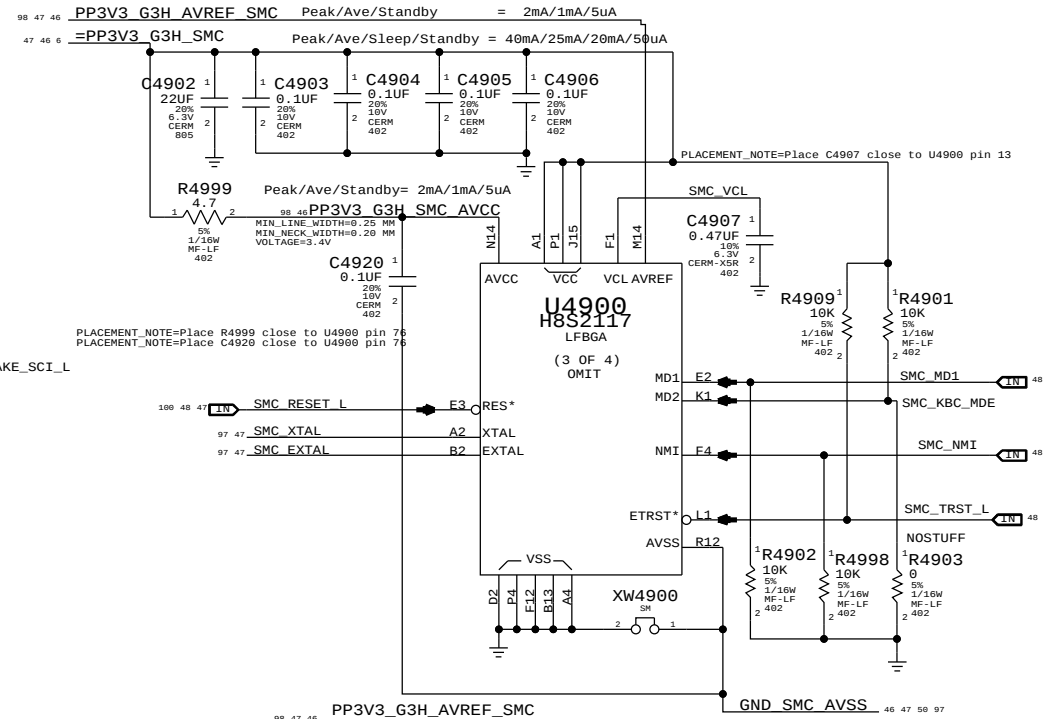
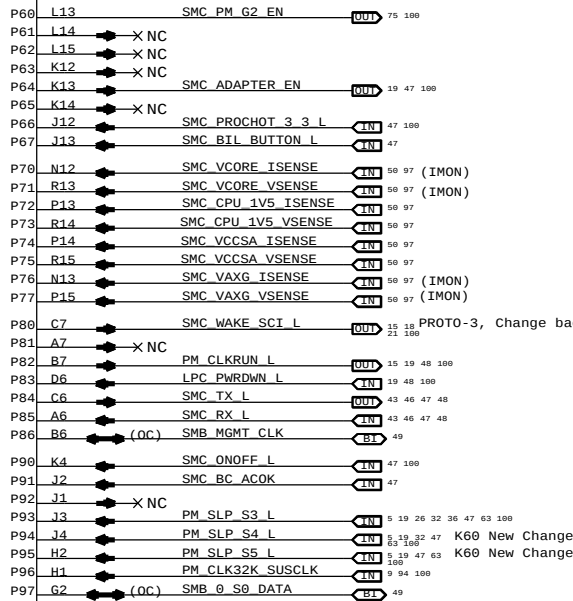
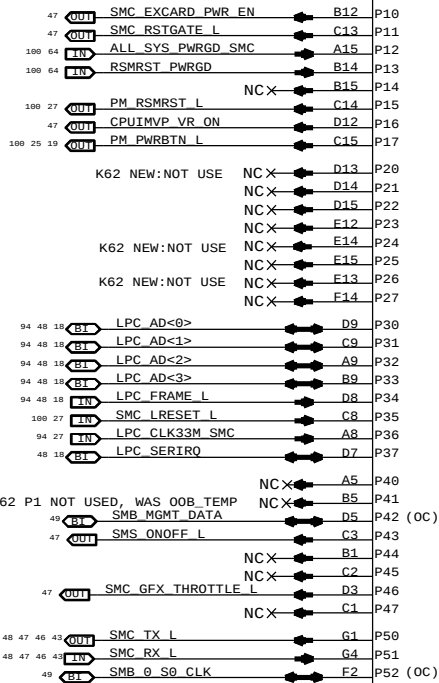




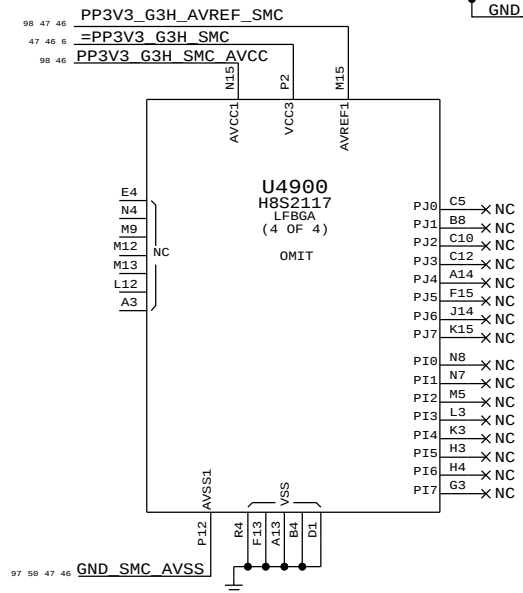
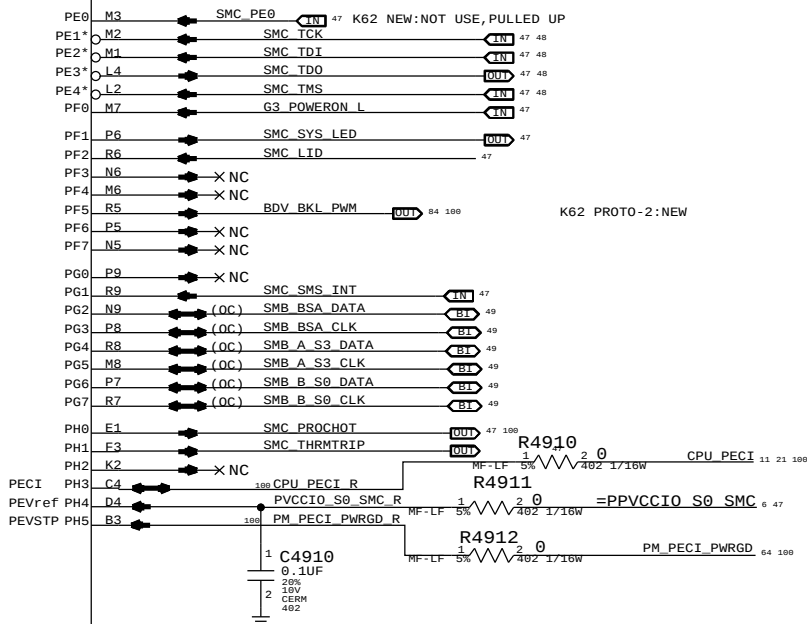
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

338S0878

U4900
H8S2117
LFBGA
(1 OF 4)
OMIT

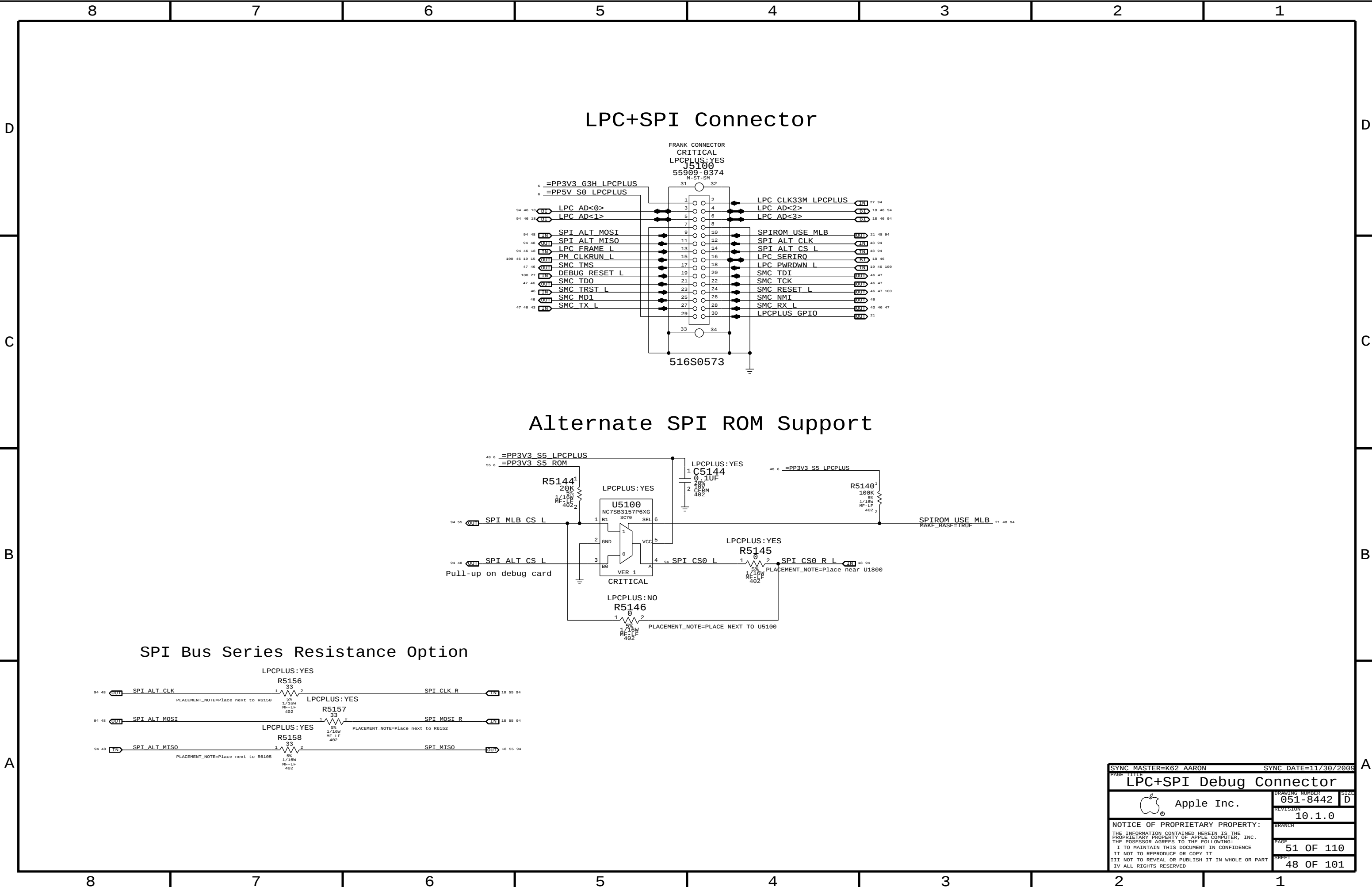


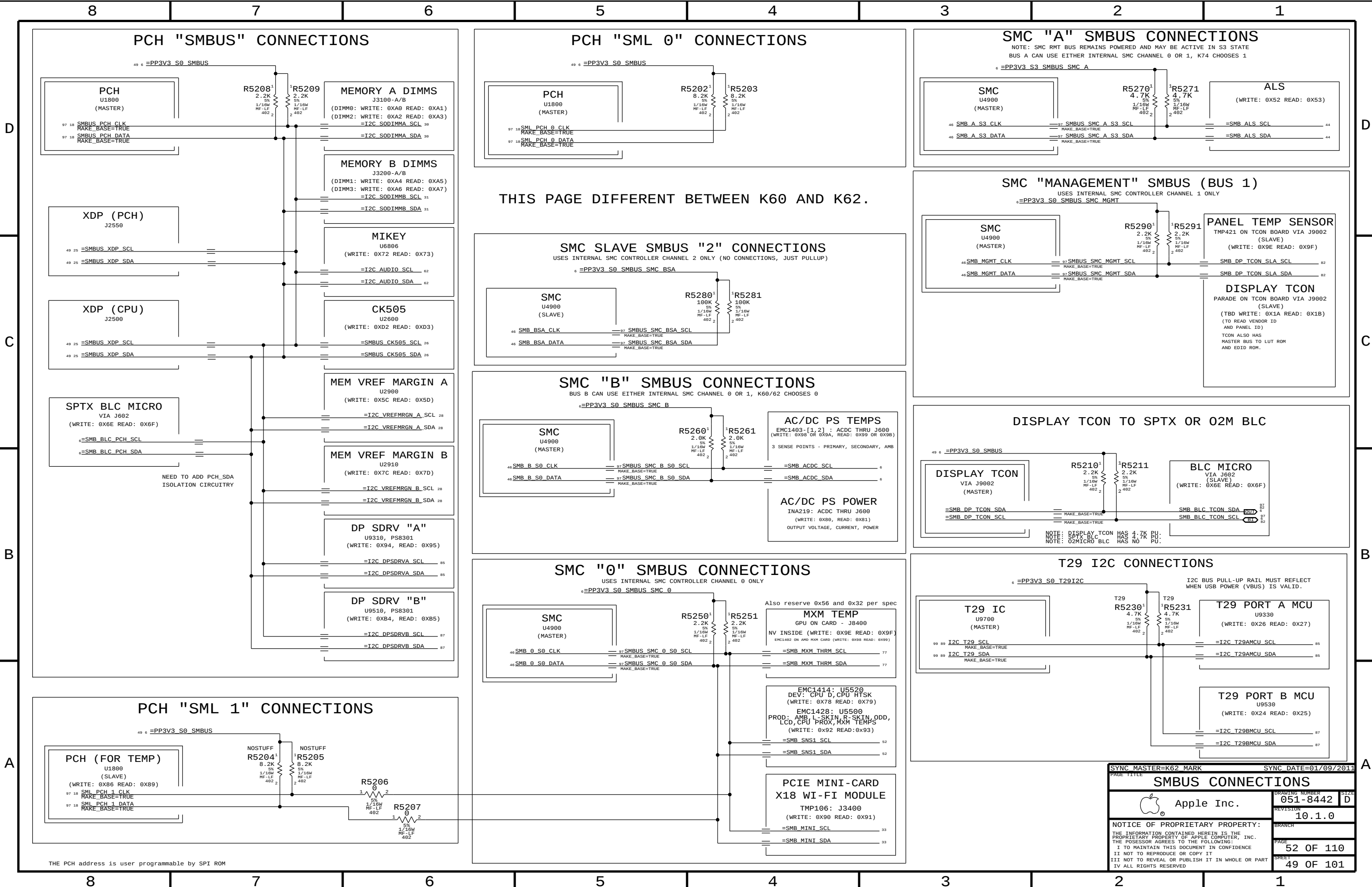
U4900
H8S2117
LFBGA
(2 OF 4)
OMIT



SMC PB3: SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)
SMC PG1: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

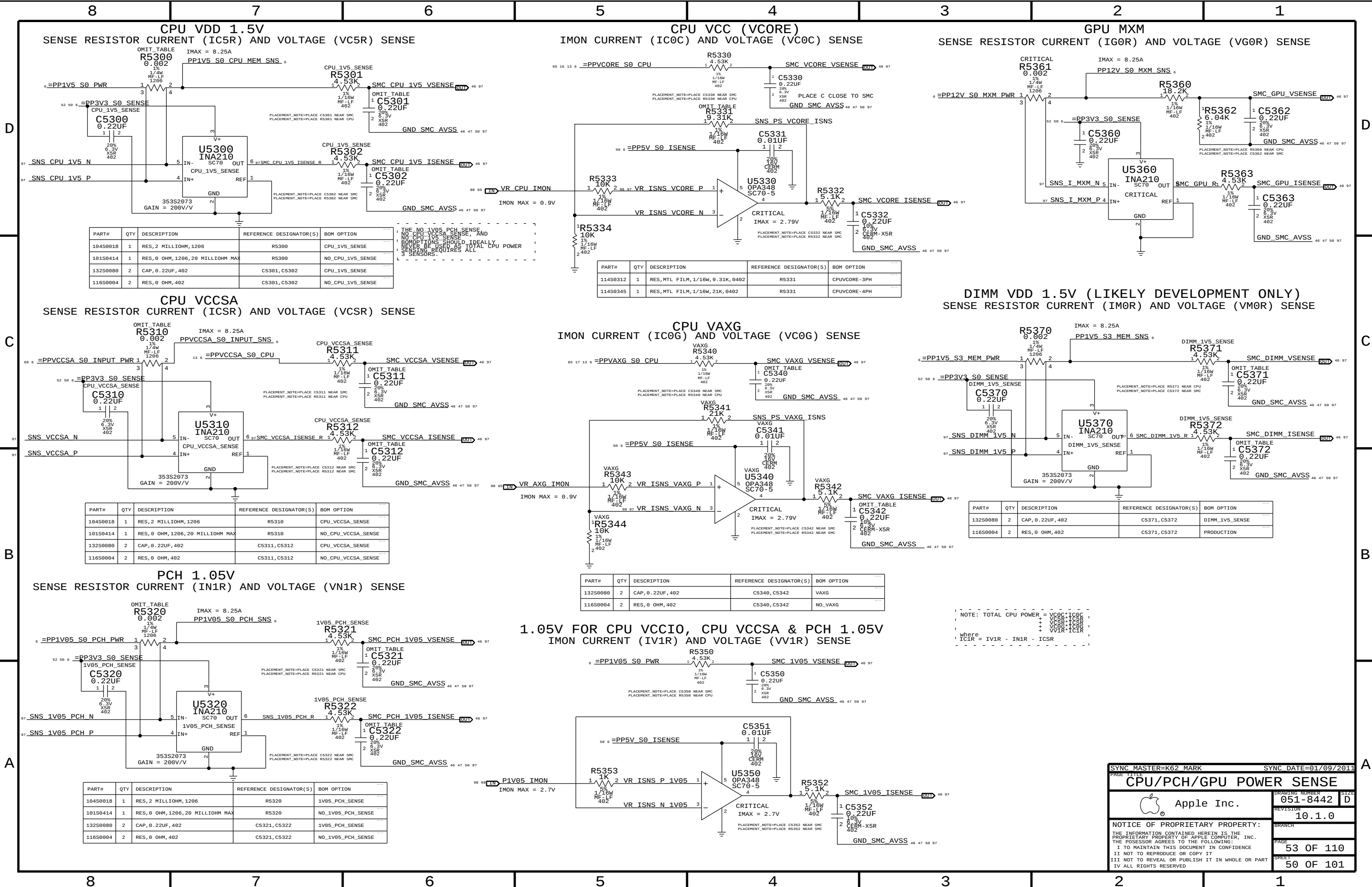
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PAGE TITLE			
SMC		DRAWING NUMBER	051-8442
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THE PCH address is user programmable by SPI ROM

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SMBUS CONNECTIONS			
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5300	CPU_1V5_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5300	NO_CPU_1V5_SENSE
132S0080	2	CAP, 0.22UF, 402	C5301, C5302	CPU_1V5_SENSE
116S0004	2	RES, 0 OHM, 402	C5301, C5302	NO_CPU_1V5_SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0312	1	RES, MTL FILM, 1/16W, 9.31K, 0402	R5331	CPUVCORE-3PH
114S0345	1	RES, MTL FILM, 1/16W, 21K, 0402	R5331	CPUVCORE-4PH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5310	CPU_VCCSA_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5310	NO_CPU_VCCSA_SENSE
132S0080	2	CAP, 0.22UF, 402	C5311, C5312	CPU_VCCSA_SENSE
116S0004	2	RES, 0 OHM, 402	C5311, C5312	NO_CPU_VCCSA_SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	2	CAP, 0.22UF, 402	C5340, C5342	VAXG
116S0004	2	RES, 0 OHM, 402	C5340, C5342	NO_VAXG

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
104S0018	1	RES, 2 MILLIOHM, 1206	R5320	1V05_PCH_SENSE
101S0414	1	RES, 0 OHM, 1206, 20 MILLIOHM MAX	R5320	NO_1V05_PCH_SENSE
132S0080	2	CAP, 0.22UF, 402	C5321, C5322	1V05_PCH_SENSE
116S0004	2	RES, 0 OHM, 402	C5321, C5322	NO_1V05_PCH_SENSE

SYNC MASTER=K62 MARK

SYNC DATE=01/09/2011

CPU/PCH/GPU POWER SENSE

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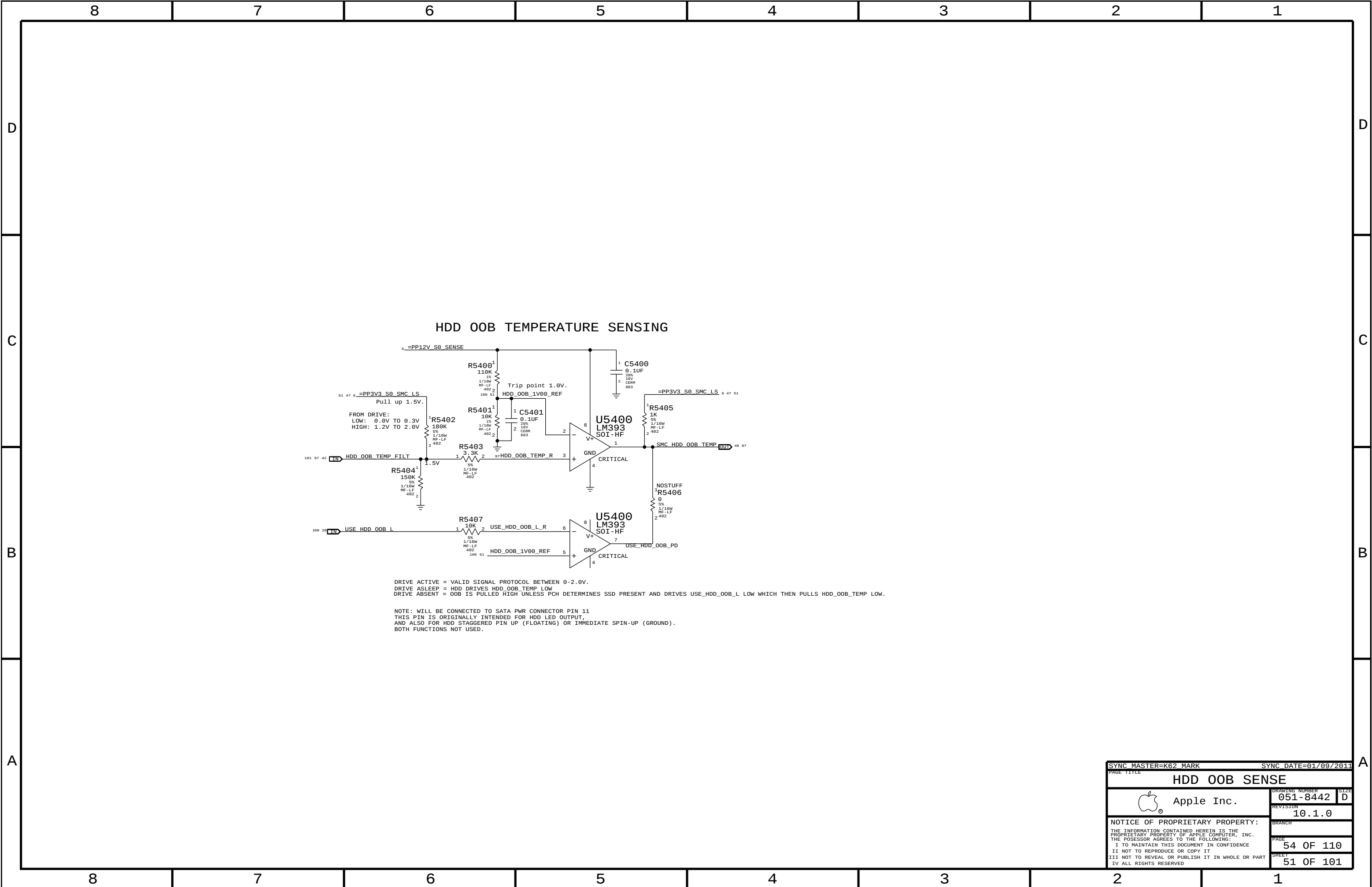
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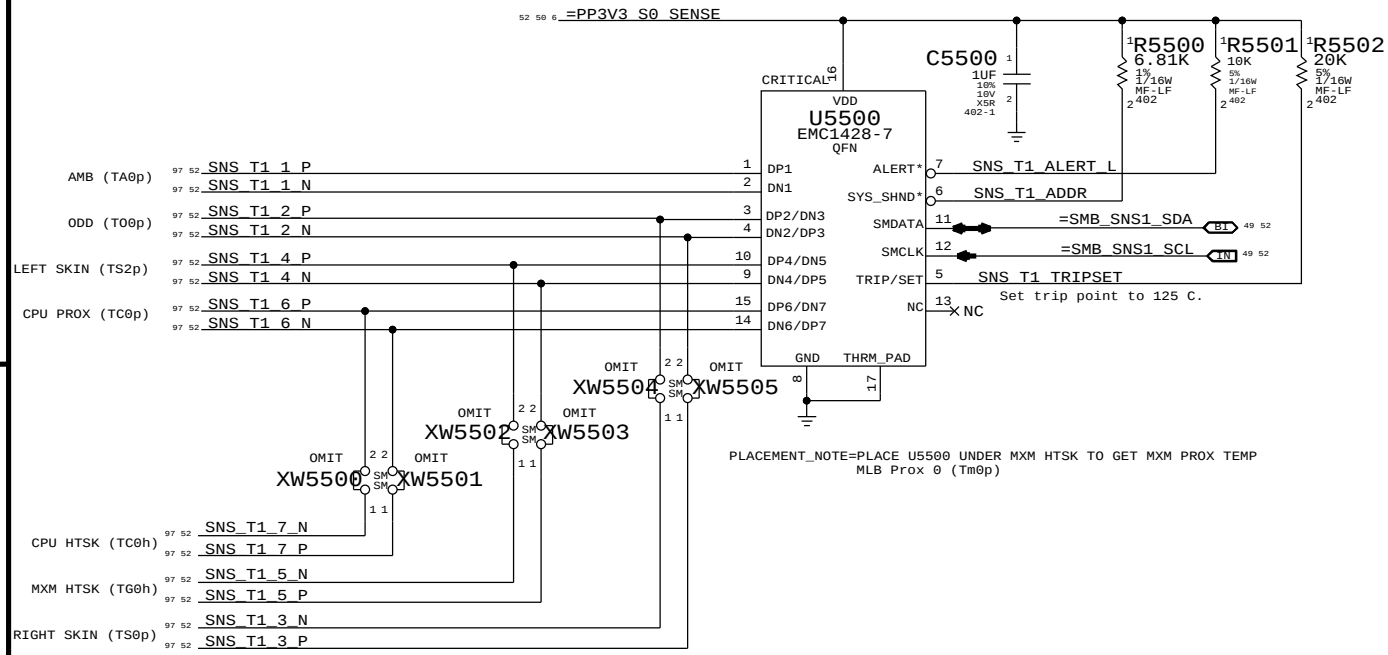
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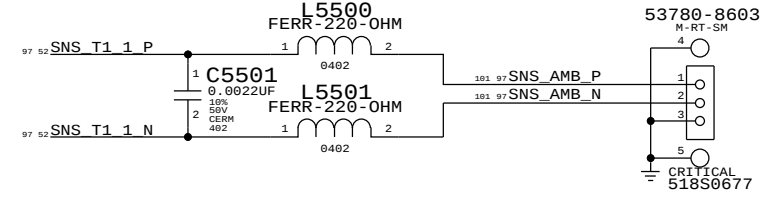


SNS T1: PRODUCTION TEMP SENSOR IC

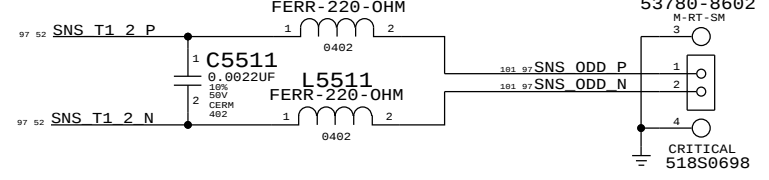


EMC1428-7: 6.8K PULL UP: I2C ADDRESS: WRITE: 0x92, READ: 0x93

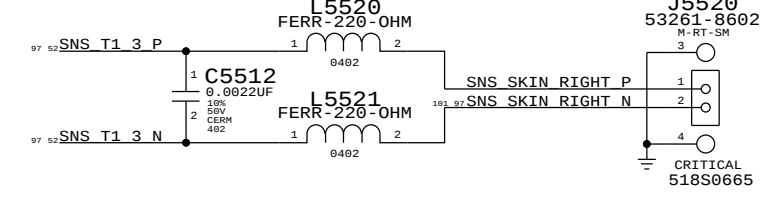
AMBIENT TEMP SENSOR



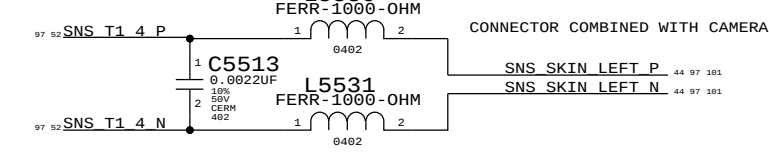
ODD TEMP SENSOR



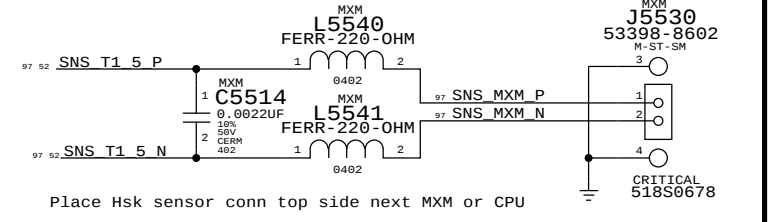
RIGHT SKIN TEMP SENSOR



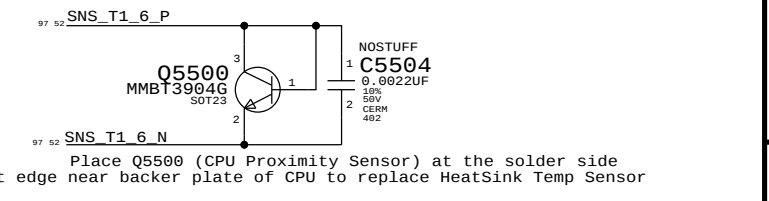
LEFT SKIN TEMP SENSOR



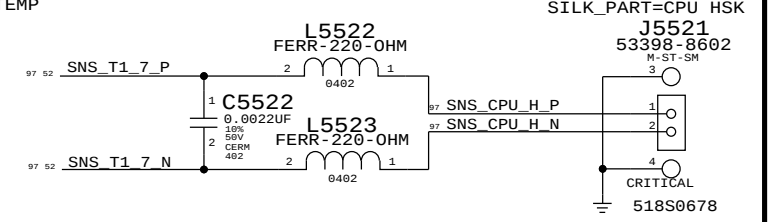
MXM HTSK TEMP SENSOR



CPU PROXIMITY TEMP SENSOR

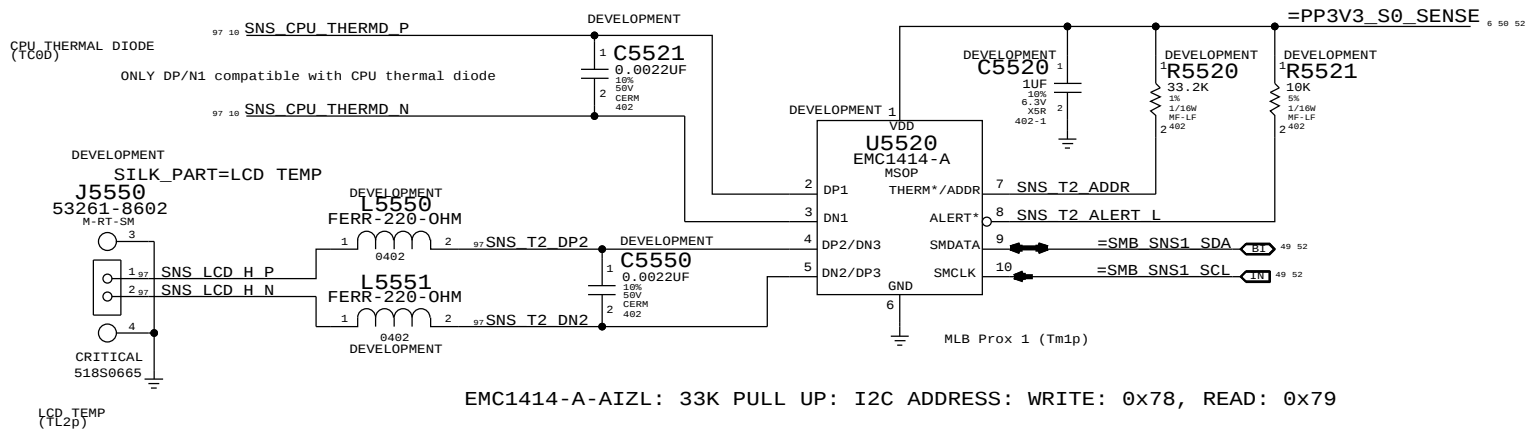


CPU HTSK TEMP SENSOR



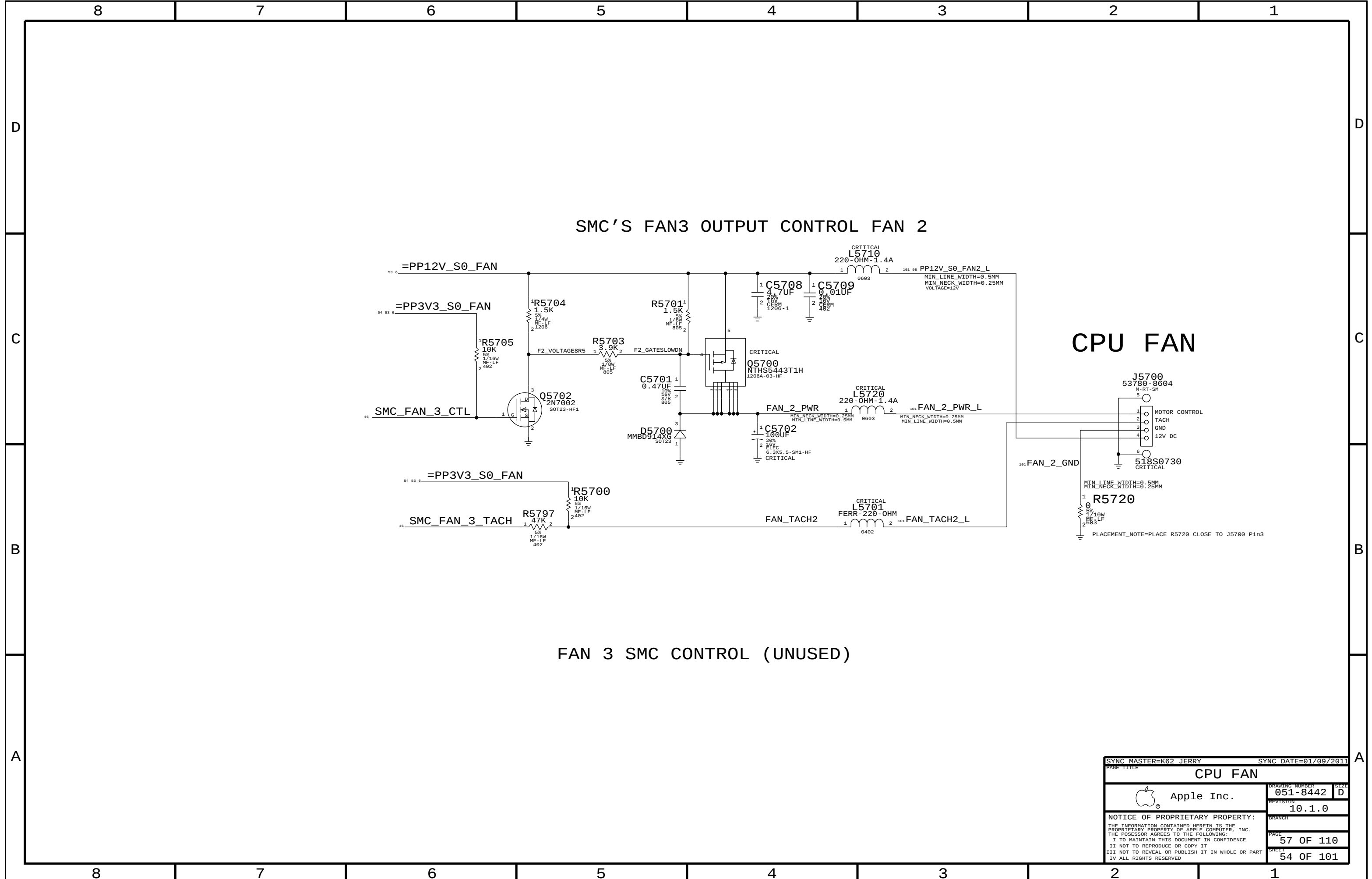
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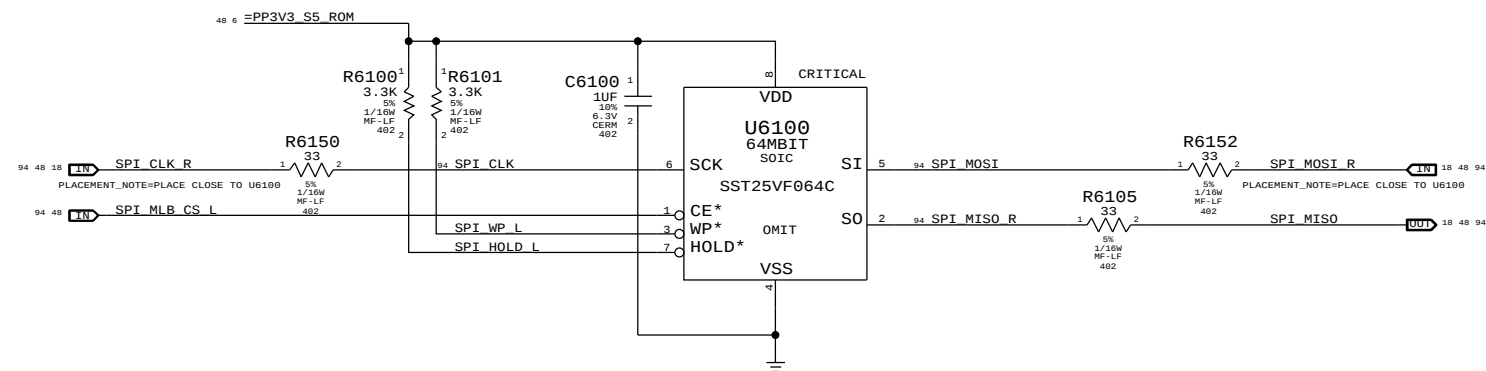


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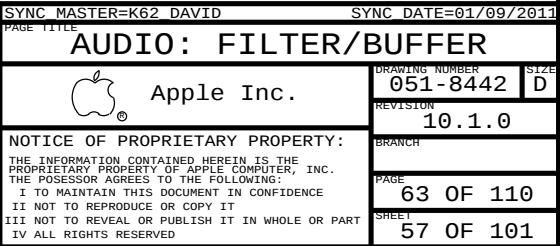
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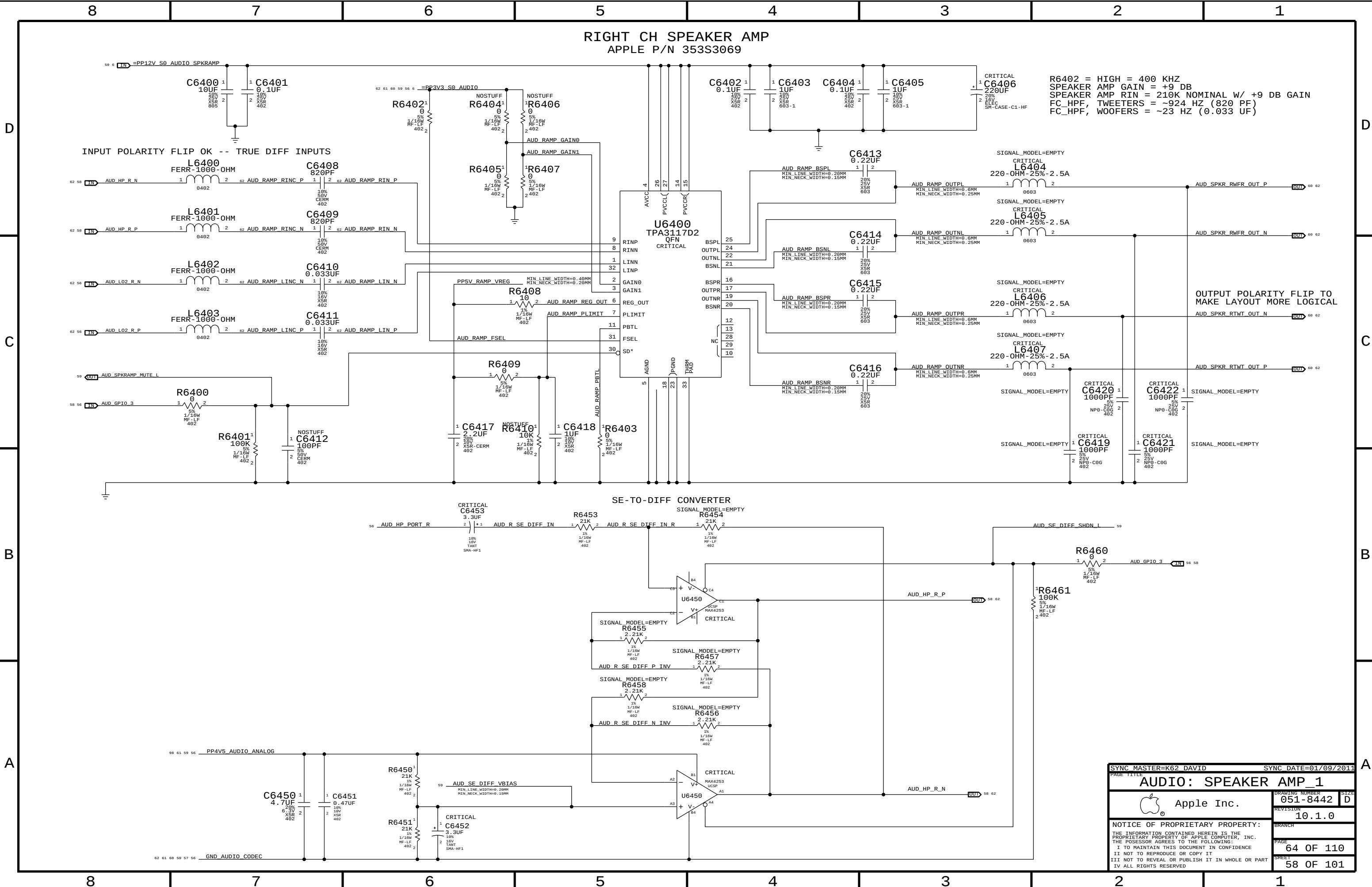


SYNC MASTER=K62 JERRY		SYNC DATE=01/09/2011	
PAGE TITLE			
CPU FAN			
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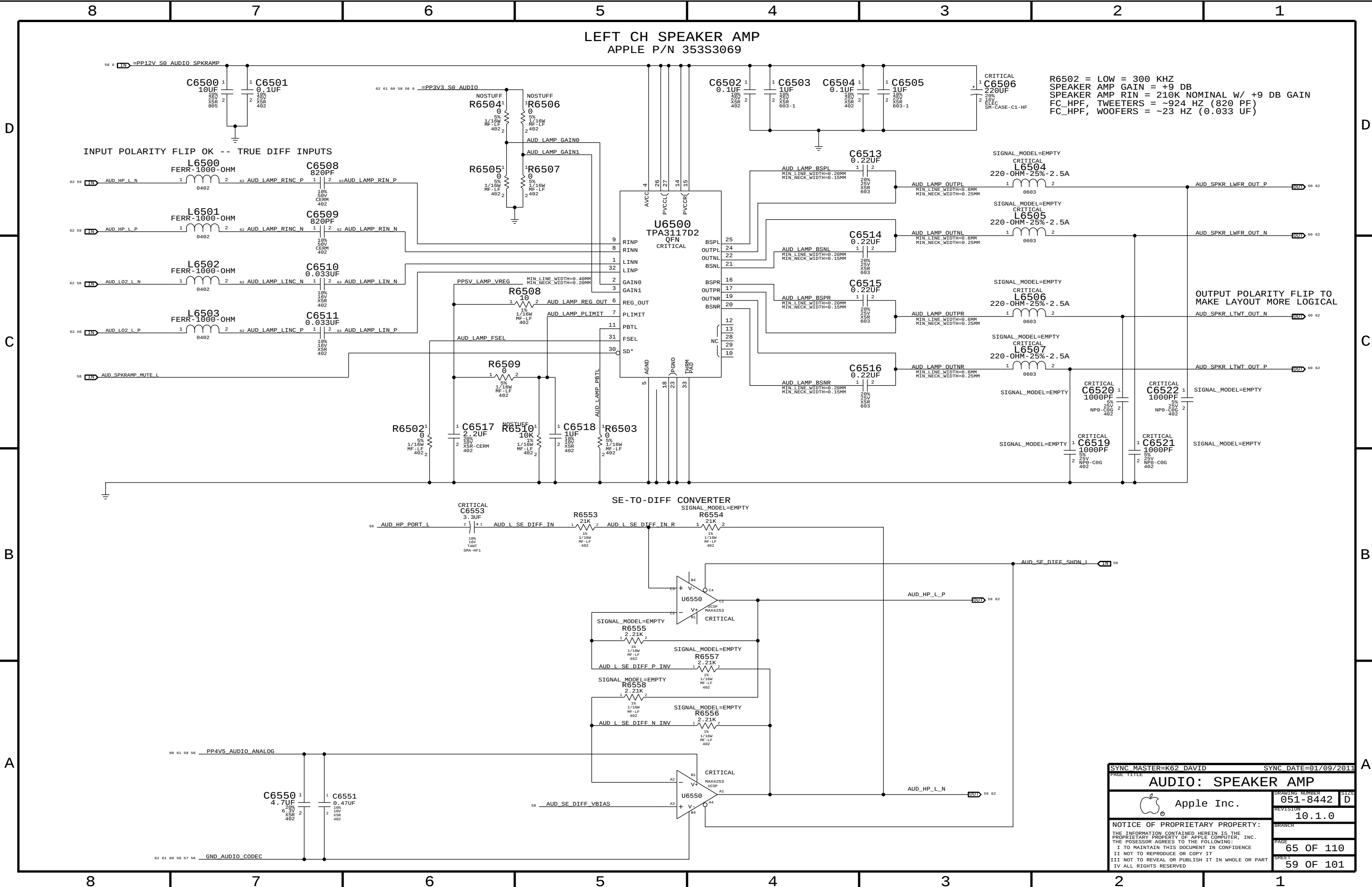


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PAGE TITLE			
SPI ROM			
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		PAGE	61 OF 110
		SHEET	
		55 OF 101	





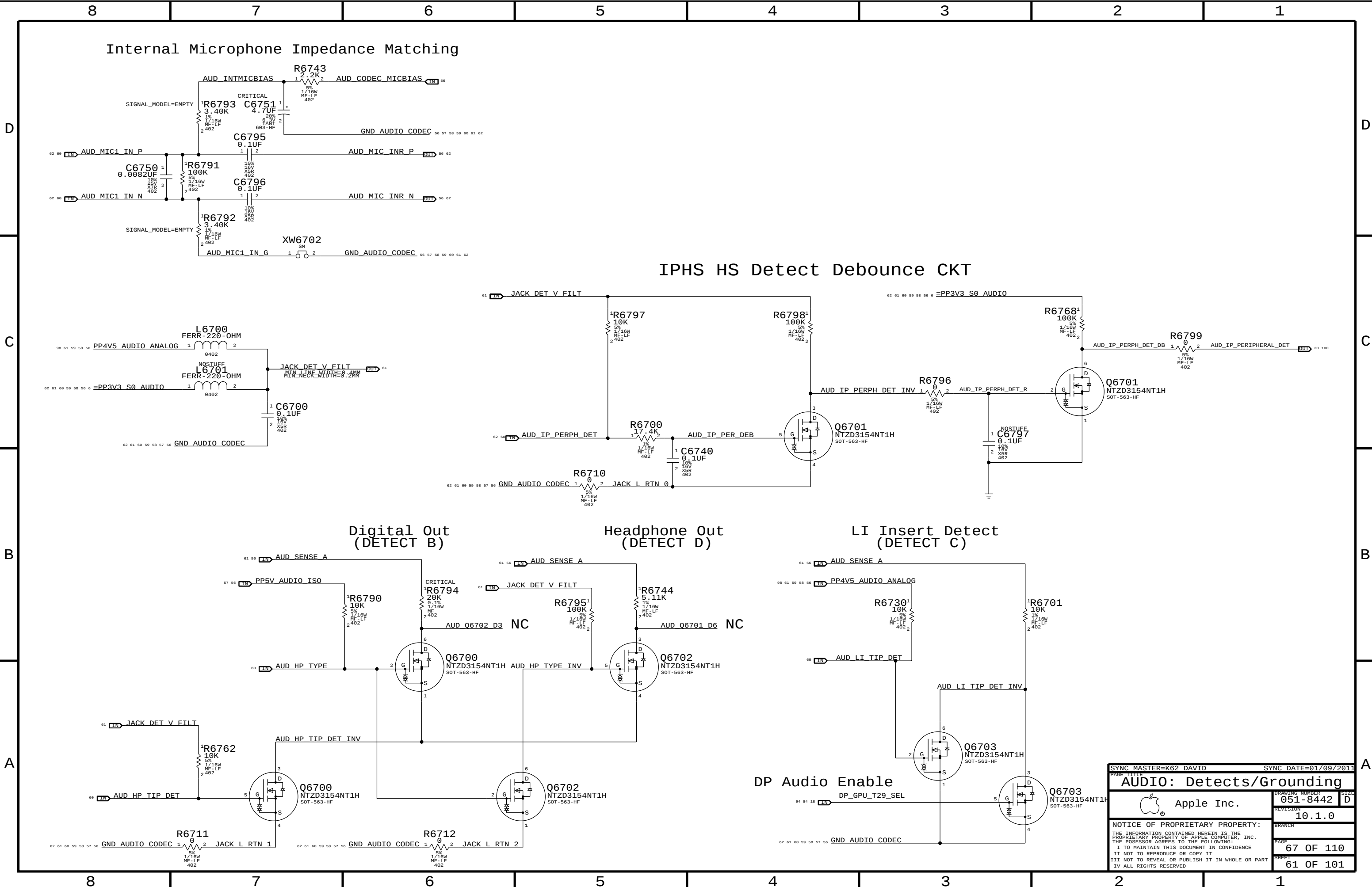
PAGE TITLE		PAGE TITLE	
AUDIO: SPEAKER AMP_1		AUDIO: SPEAKER AMP_1	
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10.1.0		10.1.0	
BRANCH		BRANCH	
PAGE		PAGE	
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58 OF 101		58 OF 101	



R6502 = LOW = 300 KHZ
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 210K NOMINAL W/ +9 DB GAIN
FC_HPF, TWEETERS = ~924 HZ (820 PF)
FC_HPF, WOOFERS = ~23 HZ (0.033 UF)

OUTPUT POLARITY FLIP TO
MAKE LAYOUT MORE LOGICAL

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PAGE TITLE		AUDIO: SPEAKER AMP	
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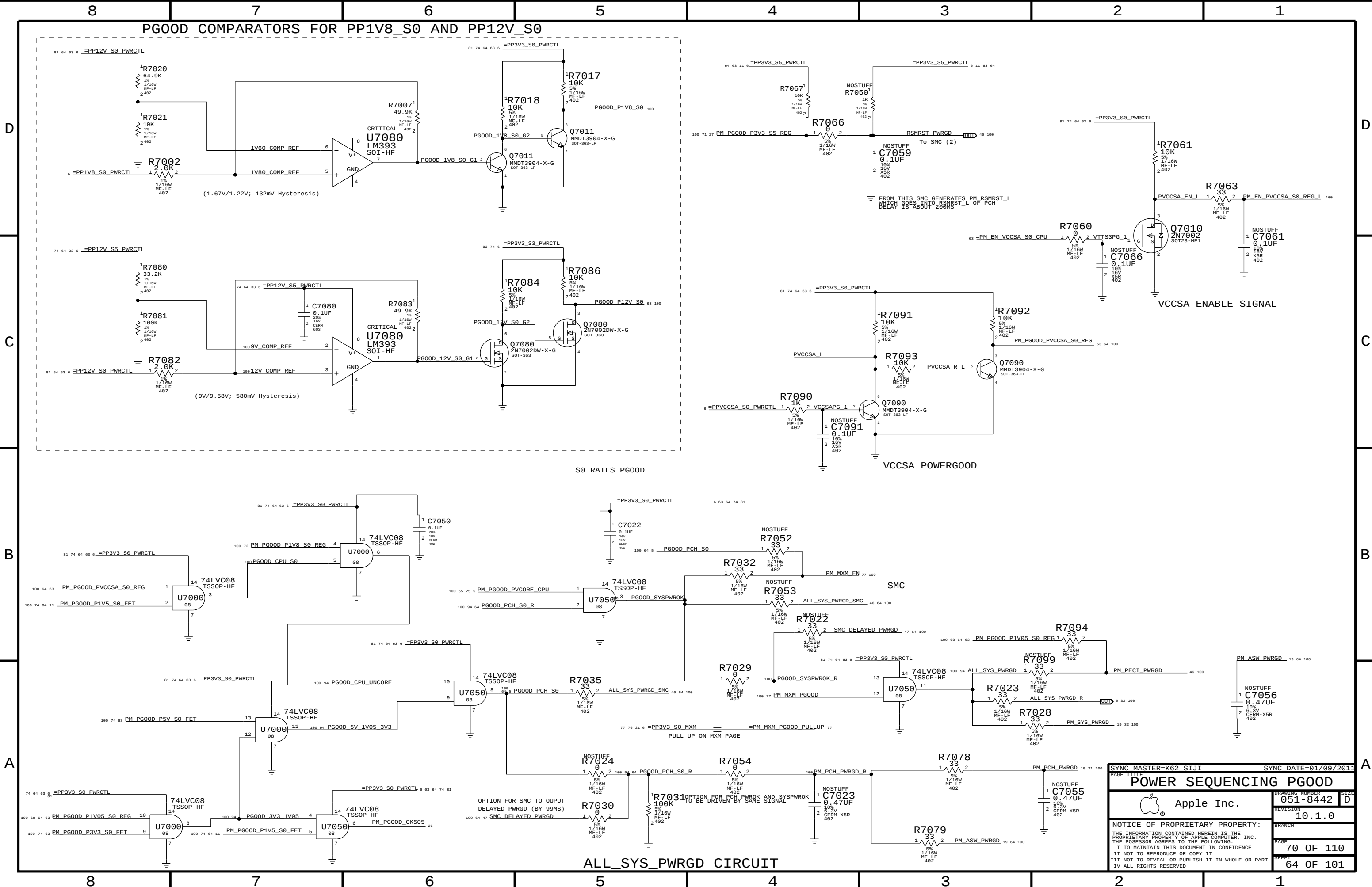
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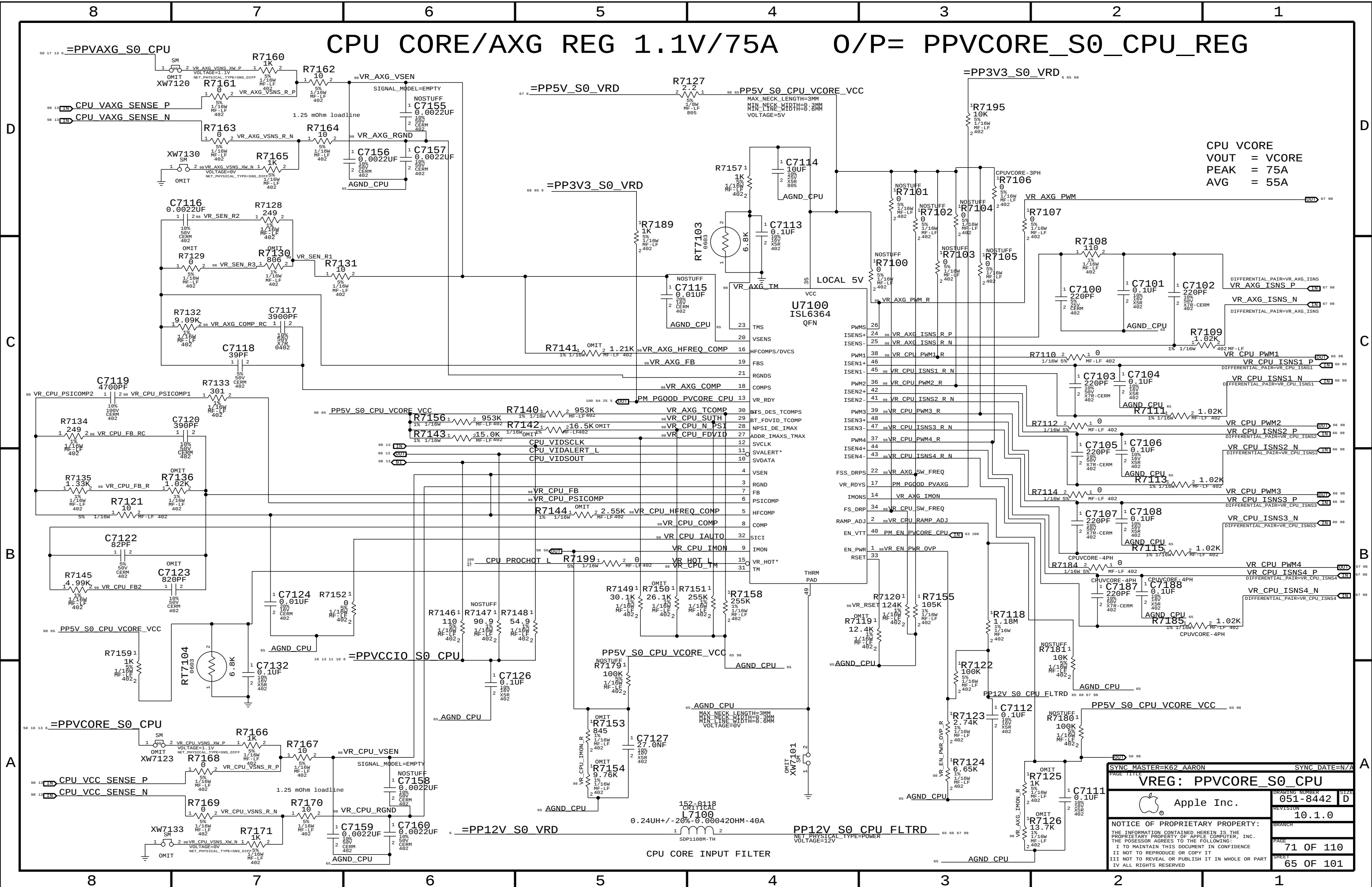
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A



PAGE TITLE		PAGE TITLE	
POWER SEQUENCING PGOOD		POWER SEQUENCING PGOOD	
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CPU CORE/AXG REG 1.1V/75A 0/P= PPVCORE_S0_CPU_REG

CPU VCORE
VOUT = VCORE
PEAK = 75A
AVG = 55A

SYNC MASTER=K62 AARON

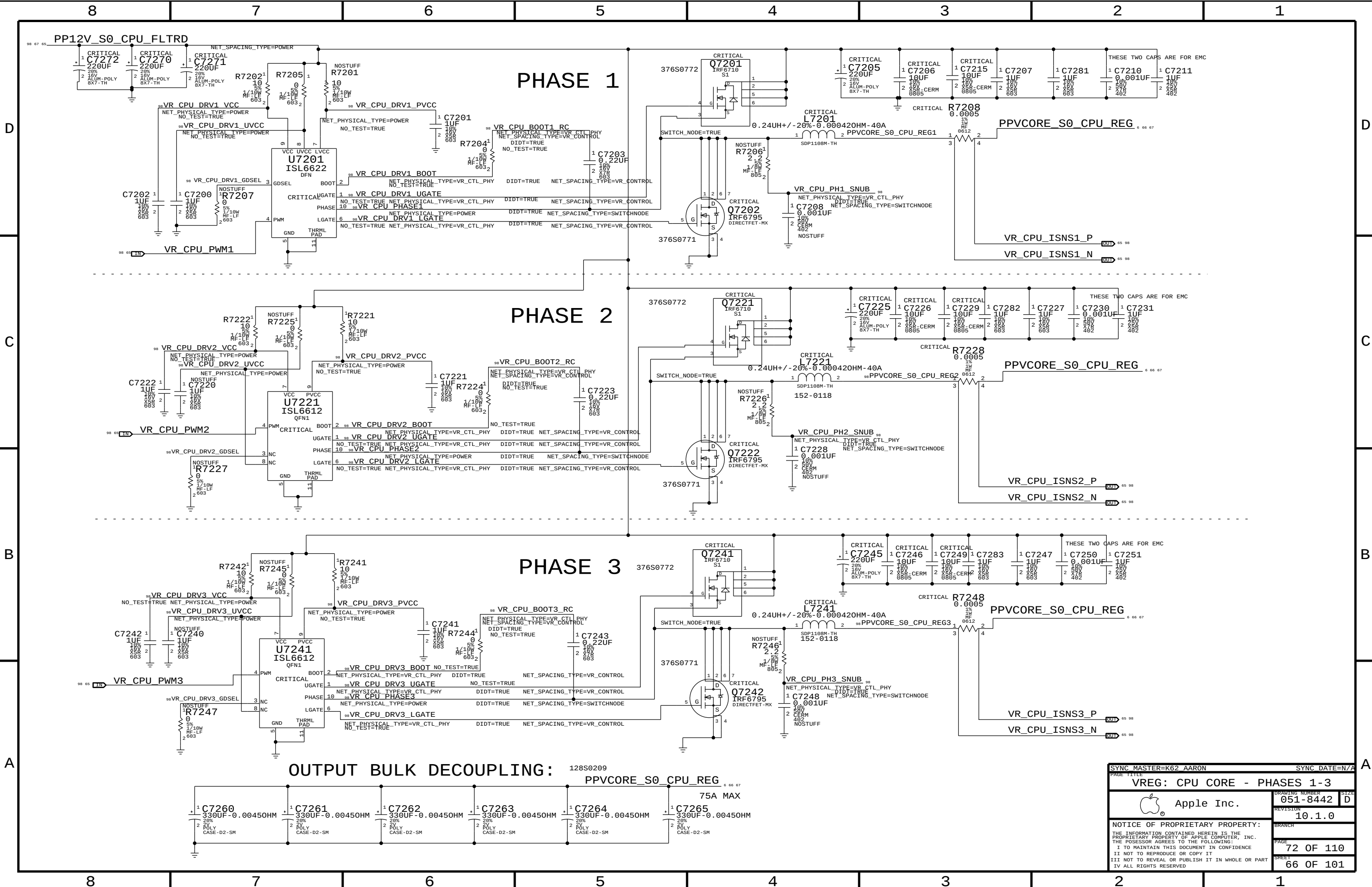
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VREG: PPVCORE_S0_CPU

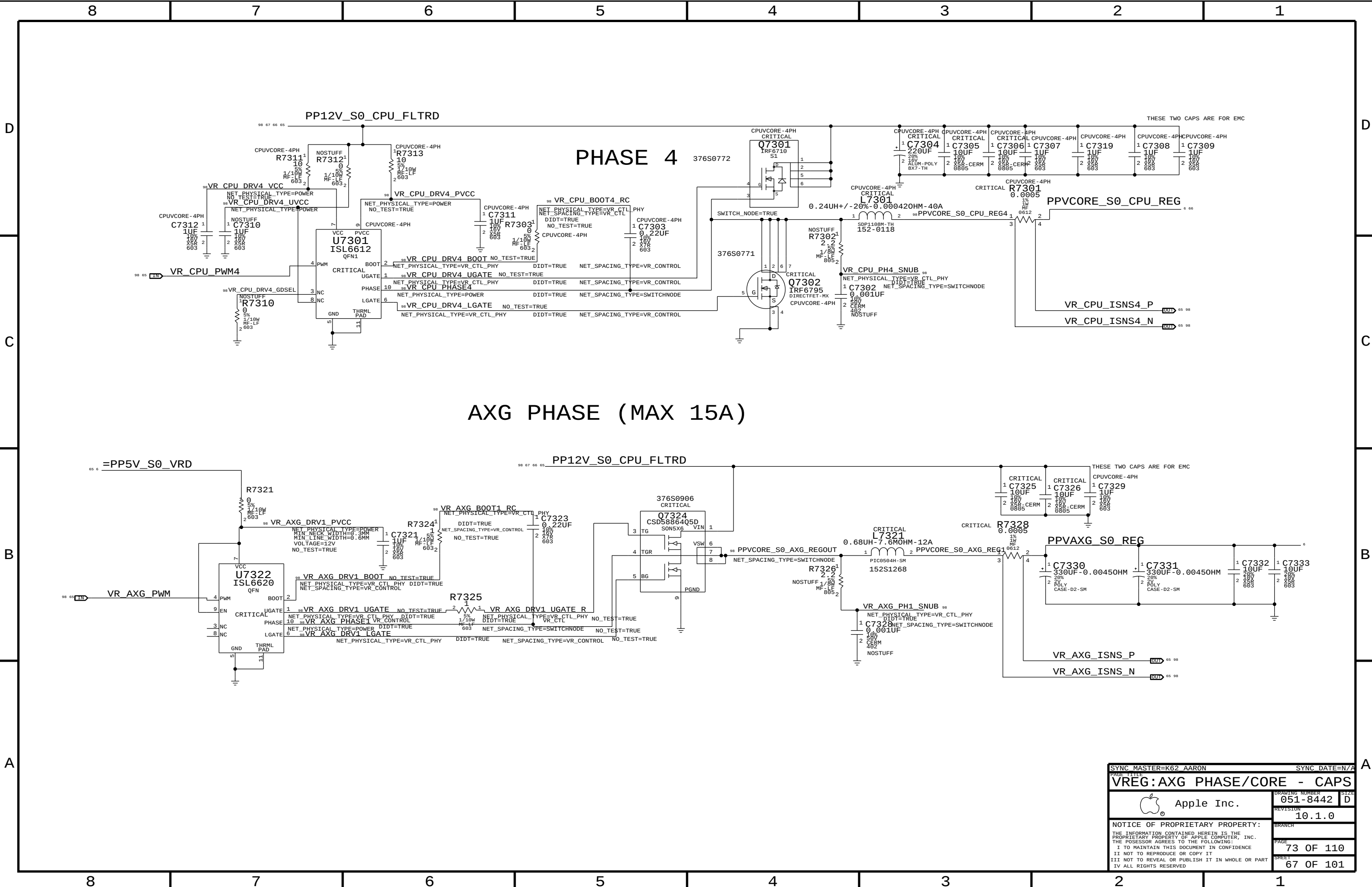
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SYNC MASTER=K62 AARON		SYNC DATE=N/A	
PAGE TITLE		VREG: CPU CORE - PHASES 1-3	
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		PAGE	72 OF 110
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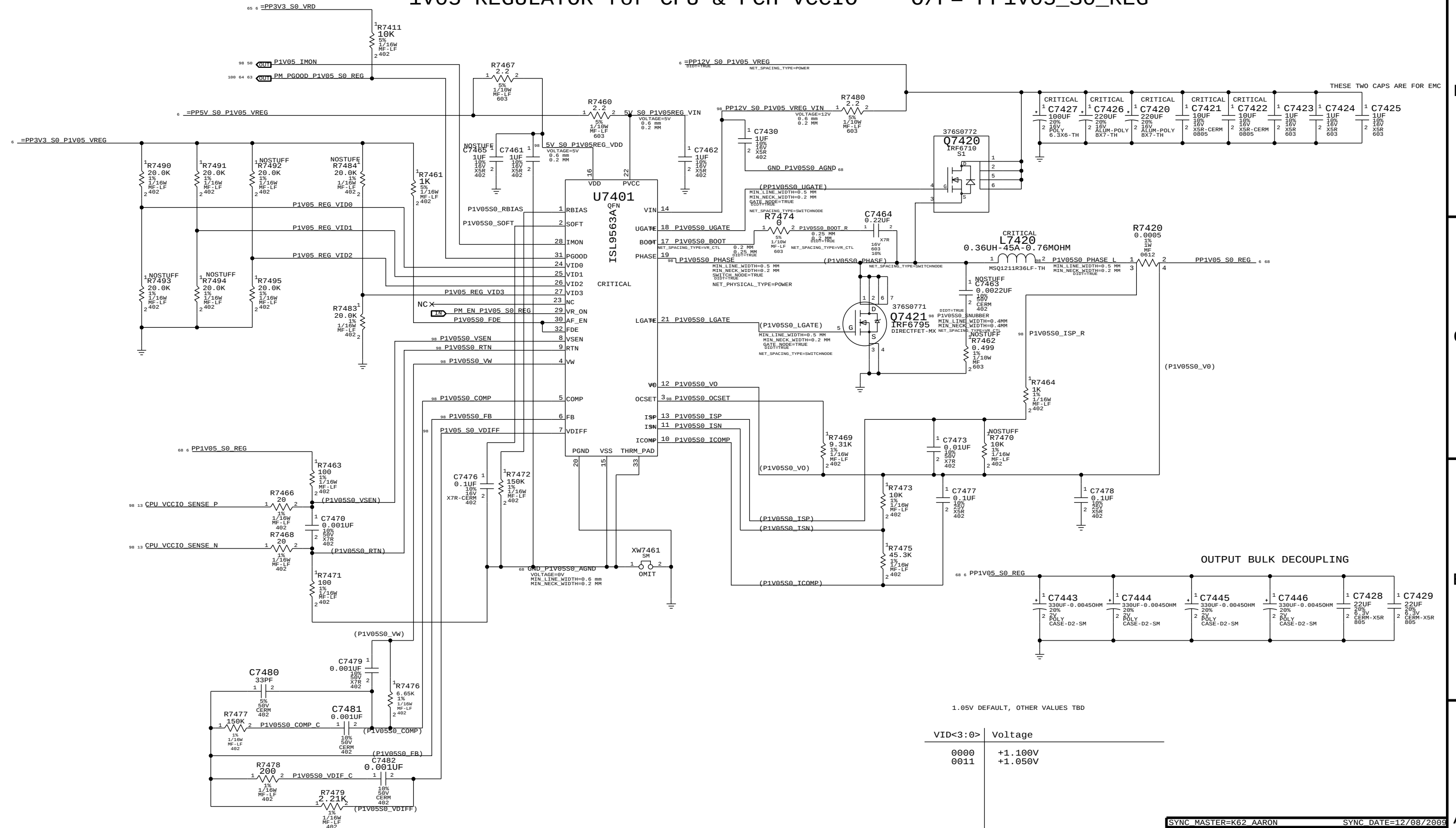


SYNC MASTER=K62 AARON		SYNC DATE=N/A	
PAGE TITLE			
VREG:AXG PHASE/CORE - CAPS			
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1V05 REGULATOR for CPU & PCH VCCIO

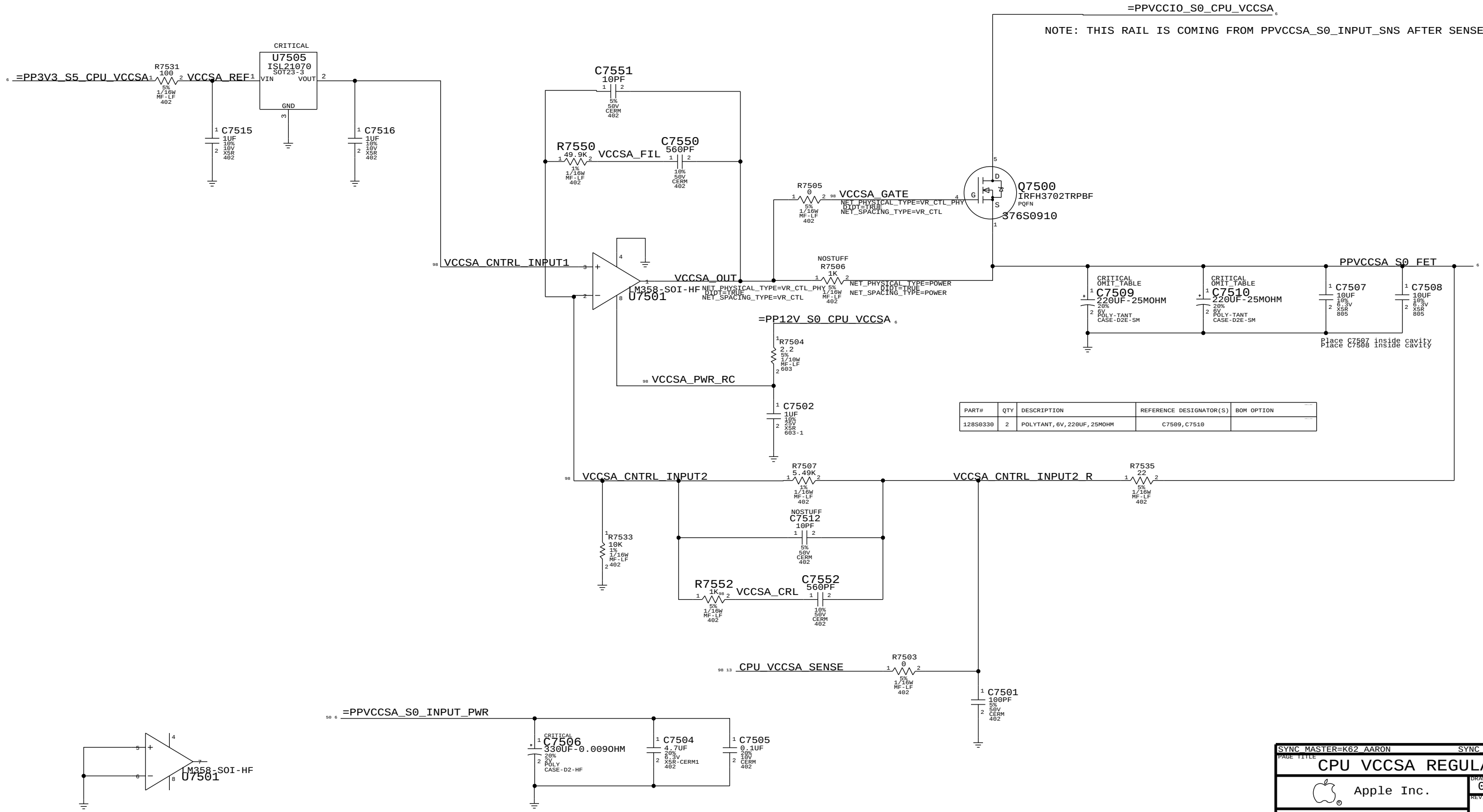
O/P= PP1V05_S0_REG



1.05V DEFAULT, OTHER VALUES TBD

VID<3:0>	Voltage
0000	+1.100V
0011	+1.050V

CPU VCCSA 0.925V (8.8A MAX)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
128S0330	2	POLYTANT, 6V, 220UF, 25MOHM	C7509, C7510	

SYNC MASTER=K62, AARON

SYNC DATE=12/08/2009

CPU VCCSA REGULATOR

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051-8442

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NOTE: THIS POWER RAIL IS BEFORE THE SENSE RES R5310

CPU VCORE 3 PHASE/4 PHASE BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0066	1	RES, 1K, 5%, 0402	R7125	CPUVCORE-4PH
114S0303	1	RES, 7.5K, 5%, 0402	R7125	CPUVCORE-3PH
114S0327	1	RES, 13.7K, 1%, 0402	R7126	CPUVCORE-4PH
114S0316	1	RES, 10.2K, 1%, 0402	R7126	CPUVCORE-3PH
114S0323	1	RES, 12.4K, 1%, 0402	R7119	CPUVCORE-4PH
114S0316	1	RES, 10.2K, 1%, 0402	R7119	CPUVCORE-3PH
114S0355	1	RES, 26.1K, 1%, 0402	R7150	CPUVCORE-4PH
114S0338	1	RES, 17.8K, 1%, 0402	R7150	CPUVCORE-3PH
114S0211	1	RES, 845, 1%, 0402	R7153	CPUVCORE-4PH
116S0004	1	RES, 0, 1%, 0402	R7153	CPUVCORE-3PH
114S0314	1	RES, 9.76K, 1%, 0402	R7154	CPUVCORE-4PH
114S0316	1	RES, 10.2K, 1%, 0402	R7154	CPUVCORE-3PH
114S0225	1	RES, 1.21K, 1%, 0402	R7141	CPUVCORE-4PH
114S0217	1	RES, 976, 1%, 0402	R7141	CPUVCORE-3PH
114S0335	1	RES, 16.5K, 1%, 0402	R7142	CPUVCORE-4PH
114S0349	1	RES, 23.2K, 1%, 0402	R7142	CPUVCORE-3PH
114S0331	1	RES, 15K, 1%, 0402	R7143	CPUVCORE-3PH
114S0257	1	RES, 2.55K, 1%, 0402	R7144	CPUVCORE-4PH
114S0252	1	RES, 2.32K, 1%, 0402	R7144	CPUVCORE-3PH
114S0209	1	RES, 806, 1%, 0402	R7130	CPUVCORE-4PH
114S0188	1	RES, 487, 1%, 0402	R7130	CPUVCORE-3PH
116S0004	1	RES, 0R, 1%, 0402	R7129	CPUVCORE-4PH
114S0189	1	RES, 499, 1%, 0402	R7129	CPUVCORE-3PH
114S0219	1	RES, 1.02K, 1%, 0402	R7136	CPUVCORE-4PH
114S0131	1	RES, 130, 1%, 0402	R7136	CPUVCORE-3PH
132S0221	1	CAP, 820PF, 10%, 0402	C7123	CPUVCORE-4PH
132S1534	1	CAP, 0.0012UF, 10%, 0402	C7123	CPUVCORE-3PH

3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

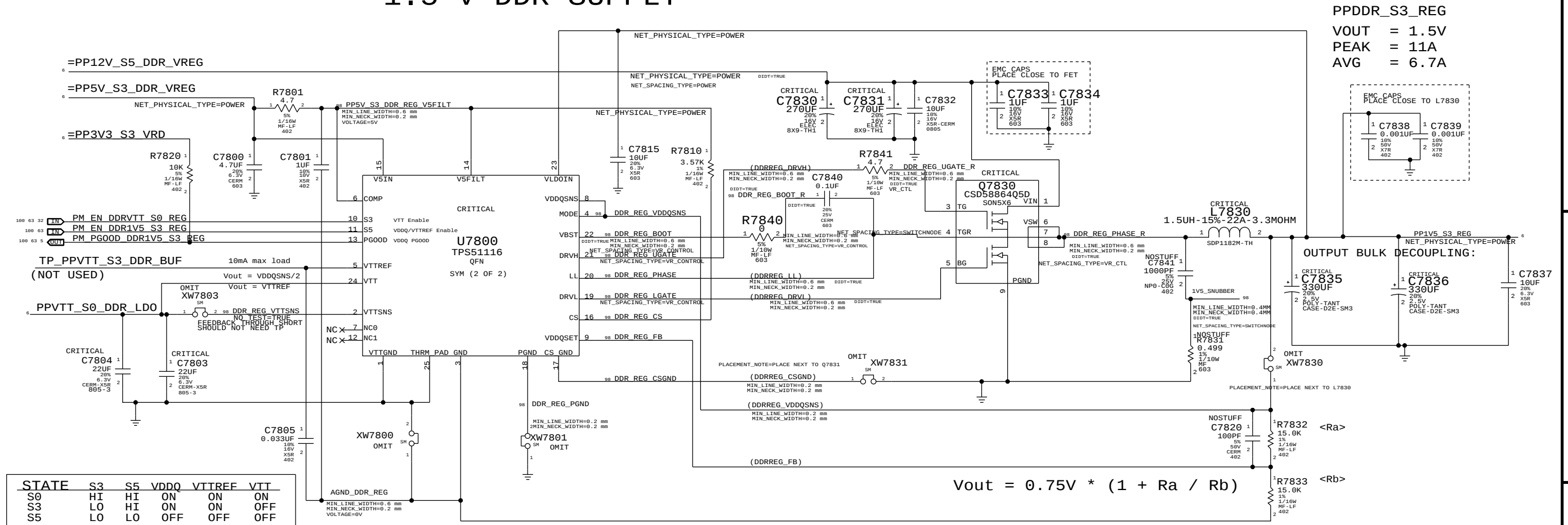
5V OUTPUT

OUTPUT BULK DECOUPLING:

$$V_{out} = 0.6V * (1 + R_a / R_b)$$

PAGE TITLE		PAGE TITLE	
5V_S3 / 3V3_S5 VREGS		DRAWING NUMBER	
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1.5 V DDR SUPPLY

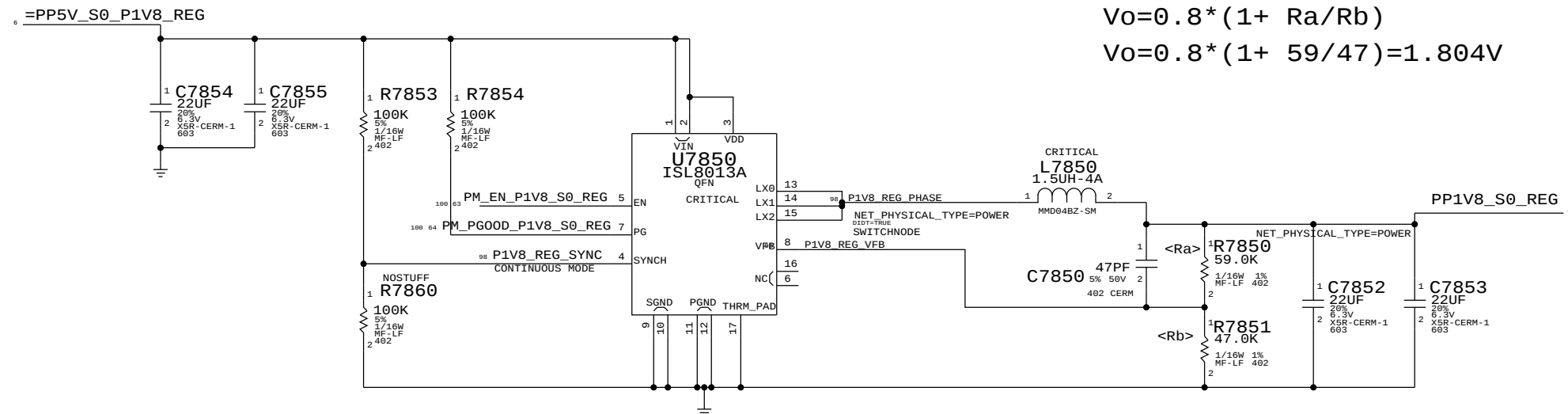


1.8 V SUPPLY

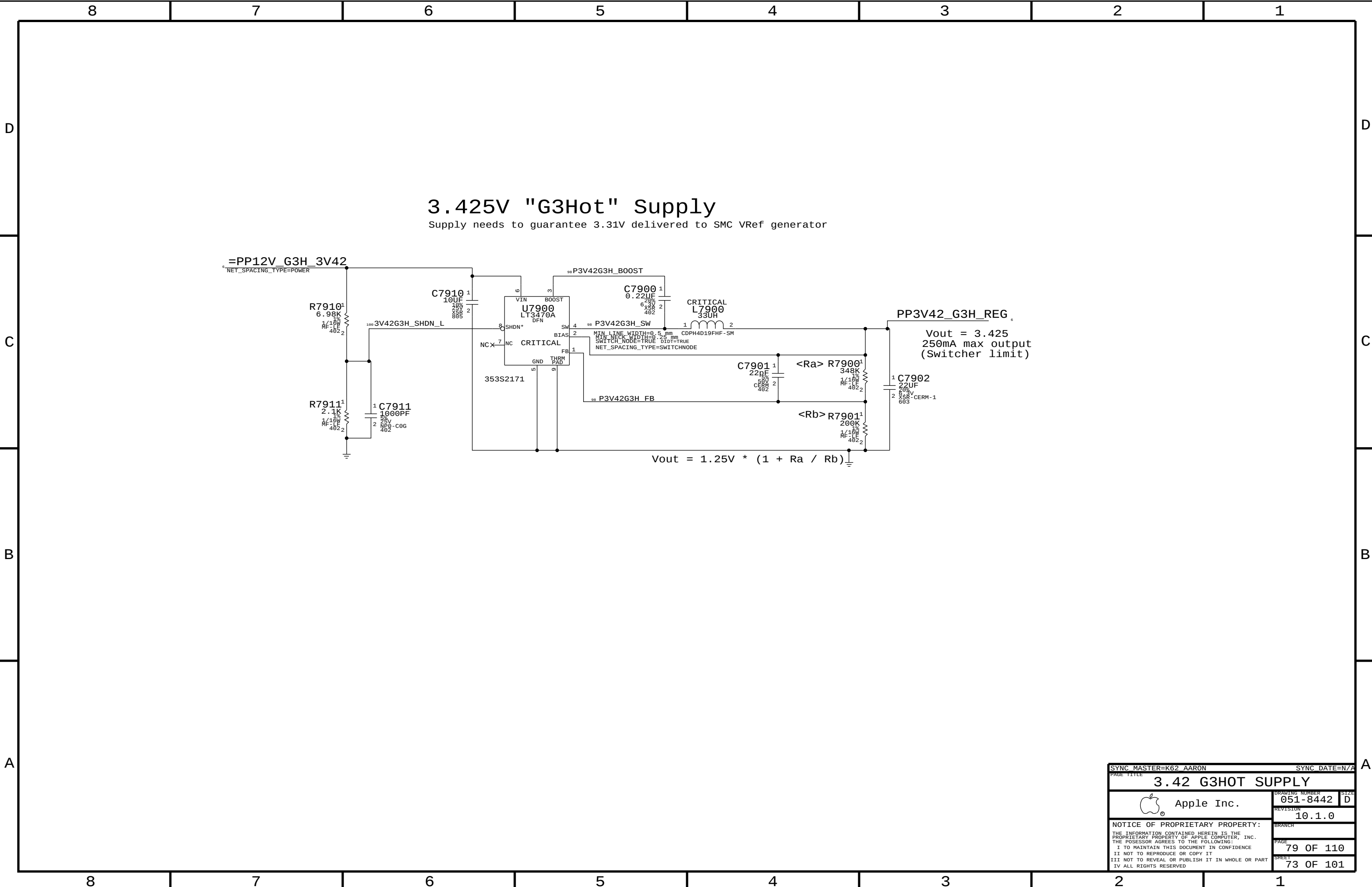
1A Average current

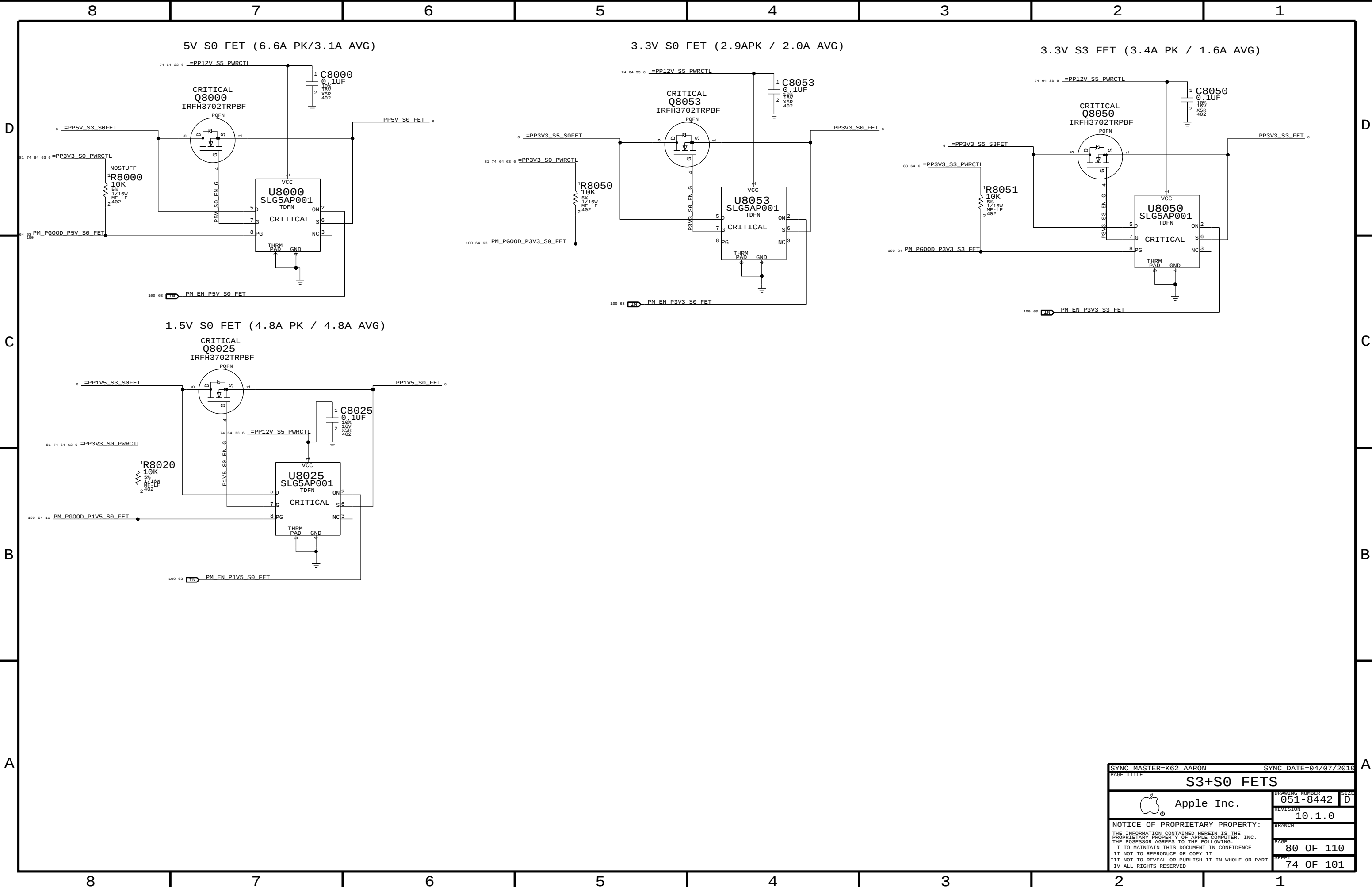
$$Vo = 0.8 * (1 + Ra/Rb)$$

$$Vo = 0.8 * (1 + 59/47) = 1.804V$$



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PAGE TITLE		1.5V / 1.8V VREGS	
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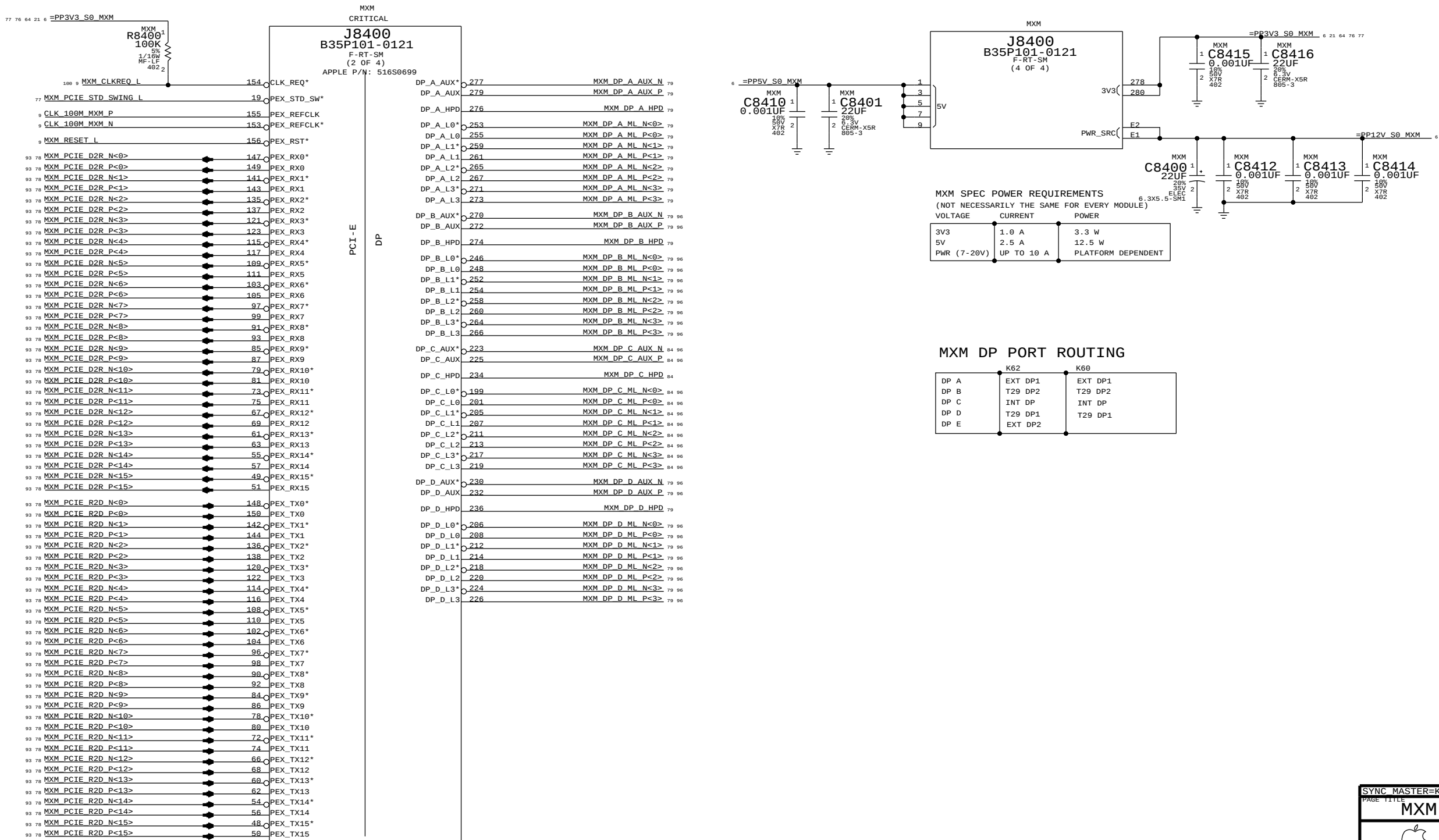
Power aliases required by this page:

- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

- MXM



SYNC MASTER=K62 AARON		SYNC DATE=N/A	
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MXM PCIe, DP & Power			
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Page Notes

Power aliases required by this page:

- =PP3V3_S0_MXM

Signal aliases required by this page:

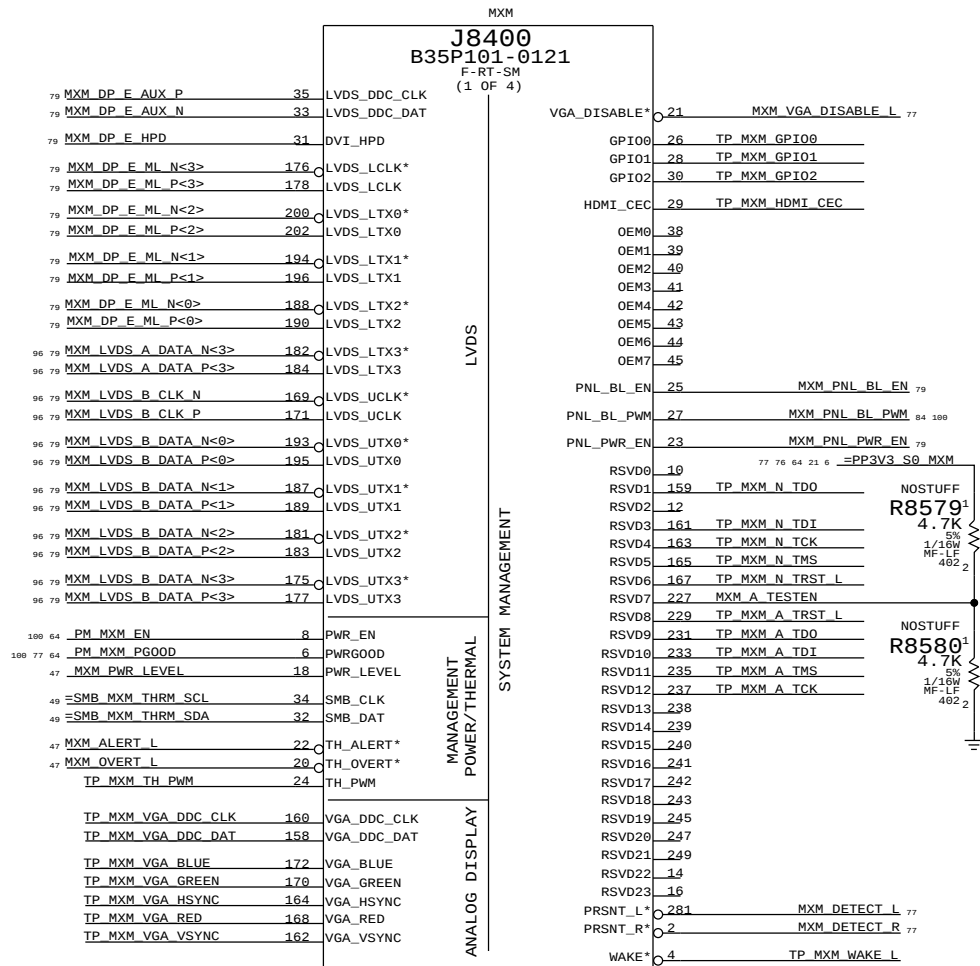
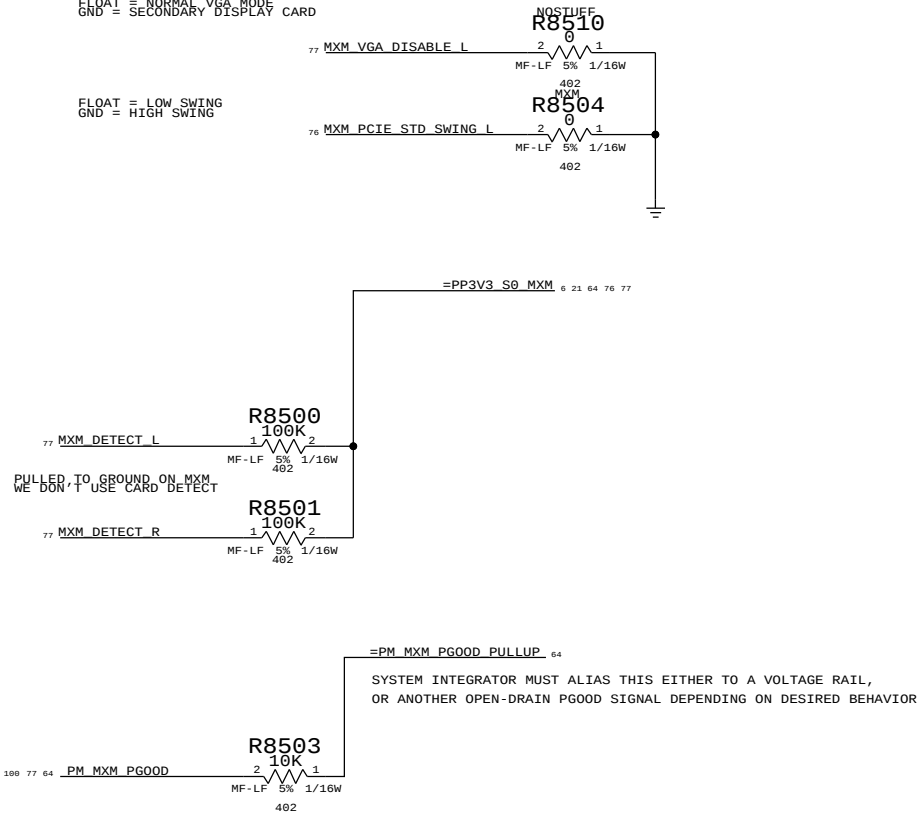
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

BOM options provided by this page:

PULLUPS & PULLEDOWNS AT MXM CONNECTOR

FLOAT = NORMAL VGA MODE
GND = SECONDARY DISPLAY CARD

FLOAT = LOW SWING
GND = HIGH SWING



SYNC MASTER=K62 AARON		SYNC DATE=N/A	
PAGE TITLE			
MXM I/O			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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		BRANCH	
		PAGE	85 OF 110
		SHEET	77 OF 101

8	7	6	5	4	3	2	1
MXM TX CAPS				MXM RX CAPS			
93	9	PEG_R2D_C_P<0>	MXM C8600 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	76	93
		PEG_R2D_C_N<0>	MXM C8601 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	76	93
93	9	PEG_R2D_C_N<1>	MXM C8602 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<14>	76	93
		PEG_R2D_C_P<1>	MXM C8603 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<14>	76	93
93	9	PEG_R2D_C_N<2>	MXM C8604 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<13>	76	93
		PEG_R2D_C_P<2>	MXM C8605 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<13>	76	93
93	9	PEG_R2D_C_P<3>	MXM C8606 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<12>	76	93
		PEG_R2D_C_N<3>	MXM C8607 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<12>	76	93
93	9	PEG_R2D_C_N<4>	MXM C8608 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<11>	76	93
		PEG_R2D_C_P<4>	MXM C8609 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<11>	76	93
93	9	PEG_R2D_C_N<5>	MXM C8610 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<10>	76	93
		PEG_R2D_C_P<5>	MXM C8611 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<10>	76	93
93	9	PEG_R2D_C_P<6>	MXM C8612 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<9>	76	93
		PEG_R2D_C_N<6>	MXM C8613 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<9>	76	93
93	9	PEG_R2D_C_N<7>	MXM C8614 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<8>	76	93
		PEG_R2D_C_P<7>	MXM C8615 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<8>	76	93
93	9	PEG_R2D_C_P<8>	MXM C8616 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<7>	76	93
		PEG_R2D_C_N<8>	MXM C8617 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<7>	76	93
93	9	PEG_R2D_C_P<9>	MXM C8618 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	76	93
		PEG_R2D_C_N<9>	MXM C8619 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<6>	76	93
93	9	PEG_R2D_C_N<10>	MXM C8620 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<5>	76	93
		PEG_R2D_C_P<10>	MXM C8621 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<5>	76	93
93	9	PEG_R2D_C_N<11>	MXM C8622 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<4>	76	93
		PEG_R2D_C_P<11>	MXM C8623 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<4>	76	93
93	9	PEG_R2D_C_P<12>	MXM C8624 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<3>	76	93
		PEG_R2D_C_N<12>	MXM C8625 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<3>	76	93
93	9	PEG_R2D_C_N<13>	MXM C8626 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<2>	76	93
		PEG_R2D_C_P<13>	MXM C8627 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<2>	76	93
93	9	PEG_R2D_C_P<14>	MXM C8628 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<1>	76	93
		PEG_R2D_C_N<14>	MXM C8629 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<1>	76	93
93	9	PEG_R2D_C_N<15>	MXM C8630 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<0>	76	93
		PEG_R2D_C_P<15>	MXM C8631 0.1UF 1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	76	93
93	76	MXM_PCIE_D2R_P<15>	MXM C8632 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<0>	9	93
		MXM_PCIE_D2R_N<15>	MXM C8633 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<0>	9	93
93	76	MXM_PCIE_D2R_P<14>	MXM C8634 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<1>	9	93
		MXM_PCIE_D2R_N<14>	MXM C8635 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<1>	9	93
93	76	MXM_PCIE_D2R_P<13>	MXM C8636 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<2>	9	93
		MXM_PCIE_D2R_N<13>	MXM C8637 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<2>	9	93
93	76	MXM_PCIE_D2R_P<12>	MXM C8638 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<3>	9	93
		MXM_PCIE_D2R_N<12>	MXM C8639 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<3>	9	93
93	76	MXM_PCIE_D2R_P<11>	MXM C8640 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<4>	9	93
		MXM_PCIE_D2R_N<11>	MXM C8641 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<4>	9	93
93	76	MXM_PCIE_D2R_P<10>	MXM C8642 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<5>	9	93
		MXM_PCIE_D2R_N<10>	MXM C8643 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<5>	9	93
93	76	MXM_PCIE_D2R_P<9>	MXM C8644 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<6>	9	93
		MXM_PCIE_D2R_N<9>	MXM C8645 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<6>	9	93
93	76	MXM_PCIE_D2R_P<8>	MXM C8646 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<7>	9	93
		MXM_PCIE_D2R_N<8>	MXM C8647 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<7>	9	93
93	76	MXM_PCIE_D2R_P<7>	MXM C8648 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<8>	9	93
		MXM_PCIE_D2R_N<7>	MXM C8649 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<8>	9	93
93	76	MXM_PCIE_D2R_P<6>	MXM C8650 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<9>	9	93
		MXM_PCIE_D2R_N<6>	MXM C8651 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<9>	9	93
93	76	MXM_PCIE_D2R_P<5>	MXM C8652 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<10>	9	93
		MXM_PCIE_D2R_N<5>	MXM C8653 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<10>	9	93
93	76	MXM_PCIE_D2R_P<4>	MXM C8654 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<11>	9	93
		MXM_PCIE_D2R_N<4>	MXM C8655 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<11>	9	93
93	76	MXM_PCIE_D2R_P<3>	MXM C8656 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<12>	9	93
		MXM_PCIE_D2R_N<3>	MXM C8657 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<12>	9	93
93	76	MXM_PCIE_D2R_P<2>	MXM C8658 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<13>	9	93
		MXM_PCIE_D2R_N<2>	MXM C8659 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<13>	9	93
93	76	MXM_PCIE_D2R_P<1>	MXM C8662 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<14>	9	93
		MXM_PCIE_D2R_N<1>	MXM C8663 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<14>	9	93
93	76	MXM_PCIE_D2R_P<0>	MXM C8660 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_N<15>	9	93
		MXM_PCIE_D2R_N<0>	MXM C8661 0.1UF 1	2 10% 16V X5R 402	PEG_D2R_P<15>	9	93

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

MXM ALIAS

76	MXM_DP_A_ML_P<0..3>	==	DP_EXTB_ML_C_P<0..3>	85	96	
			MAKE_BASE=TRUE NO_TEST=TRUE			
76	MXM_DP_A_ML_N<0..3>	==	DP_EXTB_ML_C_N<0..3>	85	96	
			MAKE_BASE=TRUE NO_TEST=TRUE			
76	MXM_DP_A_AUX_P	==	DP_EXTB_AUXCH_C_P	79	85	96
			MAKE_BASE=TRUE NO_TEST=TRUE			
76	MXM_DP_A_AUX_N	==	DP_EXTB_AUXCH_C_N	79	85	96
			MAKE_BASE=TRUE NO_TEST=TRUE			
76	MXM_DP_A_HPD	==	DP_EXTB_HPD	85		
			MAKE_BASE=TRUE NO_TEST=TRUE			
77	MXM_DP_E_ML_P<0..3>	==	DP_EXTB_ML_C_P<0..3>	87	96	
			MAKE_BASE=TRUE NO_TEST=TRUE			
77	MXM_DP_E_ML_N<0..3>	==	DP_EXTB_ML_C_N<0..3>	87	96	
			MAKE_BASE=TRUE NO_TEST=TRUE			
77	MXM_DP_E_AUX_P	==	DP_EXTB_AUXCH_C_P	79	87	96
			MAKE_BASE=TRUE NO_TEST=TRUE			
77	MXM_DP_E_AUX_N	==	DP_EXTB_AUXCH_C_N	79	87	96
			MAKE_BASE=TRUE NO_TEST=TRUE			
77	MXM_DP_E_HPD	==	DP_EXTB_HPD	87		
			MAKE_BASE=TRUE NO_TEST=TRUE			

DDC/AUX ALIAS

96	85	79	DP_EXTB_AUXCH_C_P	==	DP_EXTB_DDC_CLK	85
			MAKE_BASE=TRUE			
96	85	79	DP_EXTB_AUXCH_C_N	==	DP_EXTB_DDC_DATA	85
			MAKE_BASE=TRUE			
96	87	79	DP_EXTB_AUXCH_C_P	==	DP_EXTB_DDC_CLK	87
			MAKE_BASE=TRUE			
96	87	79	DP_EXTB_AUXCH_C_N	==	DP_EXTB_DDC_DATA	87
			MAKE_BASE=TRUE			

NO_TEST T29 & DP DC BIAS

1687	T29_A_BIAS_R2D_P0	85	86	1687	T29_B_BIAS_R2D_P2	87	88
1688	NO_TEST=TRUE			1688	NO_TEST=TRUE		
1689	T29_A_BIAS_R2D_N0	85	86	1689	T29_B_BIAS_R2D_N2	87	88
1690	NO_TEST=TRUE			1690	NO_TEST=TRUE		
1691	T29_A_BIAS_R2D_P1	85	86	1691	T29_B_BIAS_R2D_P3	87	88
1692	NO_TEST=TRUE			1692	NO_TEST=TRUE		
1693	T29_A_BIAS_R2D_N1	85	86	1693	T29_B_BIAS_R2D_N3	87	88
1694	NO_TEST=TRUE			1694	NO_TEST=TRUE		
1695	T29_A_BIAS_P0	83	85 86	1695	T29_B_BIAS_P0	83	87 88 99
1696	NO_TEST=TRUE			1696	NO_TEST=TRUE		
1697	T29_A_BIAS_P1	86		1697	T29_B_BIAS_P3	88	
1698	NO_TEST=TRUE			1698	NO_TEST=TRUE		
1699	T29_A_BIAS_N1	86		1699	T29_B_BIAS_N3	88	
1700	NO_TEST=TRUE			1700	NO_TEST=TRUE		
1701	DP_A_BIAS_P0	85	86	1701	DP_B_BIAS_P0	87	88
1702	NO_TEST=TRUE			1702	NO_TEST=TRUE		
1703	DP_A_BIAS_N0	85	86	1703	DP_B_BIAS_P2	87	88
1704	NO_TEST=TRUE			1704	NO_TEST=TRUE		
1705	DP_A_BIAS_P2	85	86	1705	DP_B_BIAS_P2	87	88
1706	NO_TEST=TRUE			1706	NO_TEST=TRUE		
1707	DP_A_BIAS_N2	85	86	1707	DP_B_BIAS_N2	87	88
1708	NO_TEST=TRUE			1708	NO_TEST=TRUE		
1709	DP_A_BIAS	85	99	1709	DP_B_BIAS	87	
1710	NO_TEST=TRUE			1710	NO_TEST=TRUE		

T29 CONN POWER AND CONTROL ALIAS

	6	=PP3V3_SW_DPAPWR	==	PP3V3_SW_DPAPWR	85	98		
	6	=PP3V3_SW_DPBAPWR	==	PP3V3_SW_DPBAPWR	87	98		
100	36	33	19	PCIE_WAKE_L	==	=T29_WAKE_L	85	87
96	76	MXM_DP_B_ML_P<0..3>	==	DP_T29SNK1_ML_C_P<0..3>	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_B_ML_N<0..3>	==	DP_T29SNK1_ML_C_N<0..3>	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_B_AUX_P	==	DP_T29SNK1_AUXCH_C_P	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_B_AUX_N	==	DP_T29SNK1_AUXCH_C_N	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
76	MXM_DP_B_HPD	==	DP_T29SNK1_HPD	89				
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_D_ML_P<0..3>	==	DP_T29SNK0_ML_C_P<0..3>	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_D_ML_N<0..3>	==	DP_T29SNK0_ML_C_N<0..3>	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_D_AUX_P	==	DP_T29SNK0_AUXCH_C_P	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
96	76	MXM_DP_D_AUX_N	==	DP_T29SNK0_AUXCH_C_N	89	99		
				MAKE_BASE=TRUE	NO_TEST=TRUE			
76	MXM_DP_D_HPD	==	DP_T29SNK0_HPD	89				
				MAKE_BASE=TRUE	NO_TEST=TRUE			

UNUSED MXM CONTROL SIGNALS

77	MXM_PNL_BL_EN	==	NC_MXM_PNL_BL_EN	MAKE_BASE=TRUE NO_TEST=TRUE
77	MXM_PNL_PWR_EN	==	NC_MXM_PNL_PWR_EN	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM Interfaces

96	77	MXM_LVDS_A_DATA_N<3>	==	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_A_DATA_P<3>	==	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_CLK_N	==	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_CLK_P	==	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_N<0>	==	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_P<0>	==	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_N<1>	==	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_P<1>	==	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_N<2>	==	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_P<2>	==	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_N<3>	==	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
96	77	MXM_LVDS_B_DATA_P<3>	==	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC MASTER=K62 AARON		SYNC DATE=N/A	
PAGE TITLE			
DP ALIAS			
 Apple Inc.		DRAWING NUMBER	051-8442
		SIZE	D
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		BRANCH	
		PAGE	87 OF 110
		SHEET	79 OF 101

GreenCLK Implementation Notes:

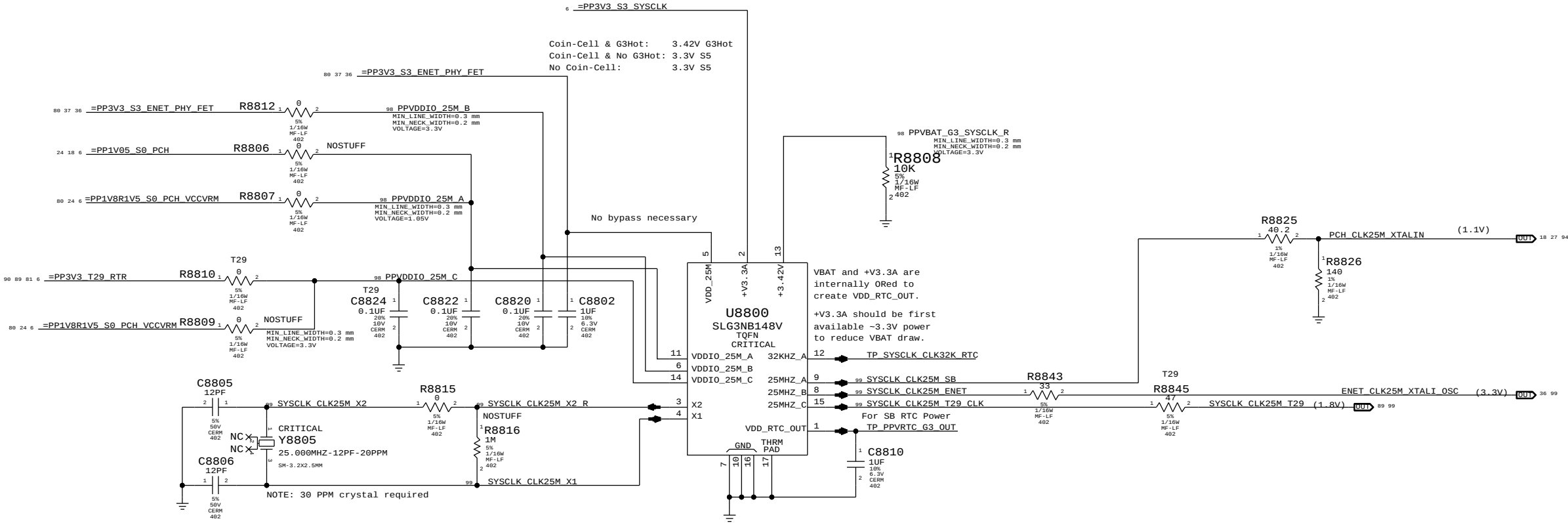
VBAT: Alias as appropriate (see note below & Desktop Example)
+V3.3A: Alias as appropriate (see note below)
VDD_25M: 3.3V matching 'highest' VDDIO power state (ENET)

VDDIO_25M_A: S8 power rail for XTAL circuit.
VDDIO_25M_B: Ethernet power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For Cougar Point Desktop: VDDIO = VCCVRM (1.8V), Vclk = 1.1V Max, Divider: 694 / 1090
For Cougar Point Mobile: VDDIO = VCCVRM (1.5V), Vclk = 1.1V Max, Divider: 332 / 1090
For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

System RTC Power Source & 32kHz / 25MHz Clock Generator



8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:

- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:

- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:

(NONE)

Supervisor & CLKREQ# Isolation

T29 CLKREQ# ISOLATION

Platform (PCIe) Reset

Open-Drain GPIO

T29_CLKREQ_FET_L

Pull-up provided by SB page.

3.3V T29 Switch

1.05V T29 Switch

T29_PWR_EN

T29

Q8950

SSM3K15FV

S0D-VESM-HF

R8904

10K

5% 1/16W NF-LF 402

R8906

10K

5% 1/16W NF-LF 402

R8907

100K

5% 1/16W NF-LF 402

R8903

10K

5% 1/16W NF-LF 402

C8900

0.1uF

18V XSR 402

C8910

1uF

10% 6.3V CERM 402

U8900

SLG4AP016V

TDFH

U8910

TPS22924

CSP

U8930

SLG5AP001

TDFN

Q8930

BSZ035N03MSG

P-TSDSON-8

PP3V3_T29_RTR

PP1V05_T29

T29_RESET_RTR_L

T29_CLKREQ_L

T29_CLKREQ_ISOL_L

MAKE_BASE=TRUE

PP3V3_S0_P3V3T29FET

PP3V3_T29_FET

Max Current = 1.7A (85C)

U8910

Part

TPS22924C

Type

Load Switch

R(on)

18 mOhm Typ

50 mOhm Max

Max Output: 2A

PP12V_S0_PWRCTL

PP1V05_S0_P1V05T29FET

PP3V3_S0_PWRCTL

PP1V05_T29_FET

PM_PG00D_P1V05_S0_T29_FET

8 7 6 5 4 3 2 1

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Page Notes

Power aliases required by this page:

- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:

- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:

(NONE)

Supervisor & CLKREQ# Isolation

T29 CLKREQ# ISOLATION

Platform (PCIe) Reset

Open-Drain GPIO

T29_CLKREQ_FET_L

Pull-up provided by SB page.

3.3V T29 Switch

1.05V T29 Switch

T29_PWR_EN

T29

Q8950

SSM3K15FV

S0D-VESM-HF

R8904

10K

5% 1/16W NF-LF 402

R8906

10K

5% 1/16W NF-LF 402

R8907

100K

5% 1/16W NF-LF 402

R8903

10K

5% 1/16W NF-LF 402

C8900

0.1uF

18V XSR 402

C8910

1uF

10% 6.3V CERM 402

U8900

SLG4AP016V

TDFH

U8910

TPS22924

CSP

U8930

SLG5AP001

TDFN

Q8930

BSZ035N03MSG

P-TSDSON-8

PP3V3_T29_RTR

PP1V05_T29

T29_RESET_RTR_L

T29_CLKREQ_L

T29_CLKREQ_ISOL_L

MAKE_BASE=TRUE

PP3V3_S0_P3V3T29FET

PP3V3_T29_FET

Max Current = 1.7A (85C)

Max Output: 2A

PP12V_S0_PWRCTL

PP1V05_S0_P1V05T29FET

PP3V3_S0_PWRCTL

PP1V05_S0_T29_EN

PP1V05_T29_FET

PM_PG00D_P1V05_S0_T29_FET

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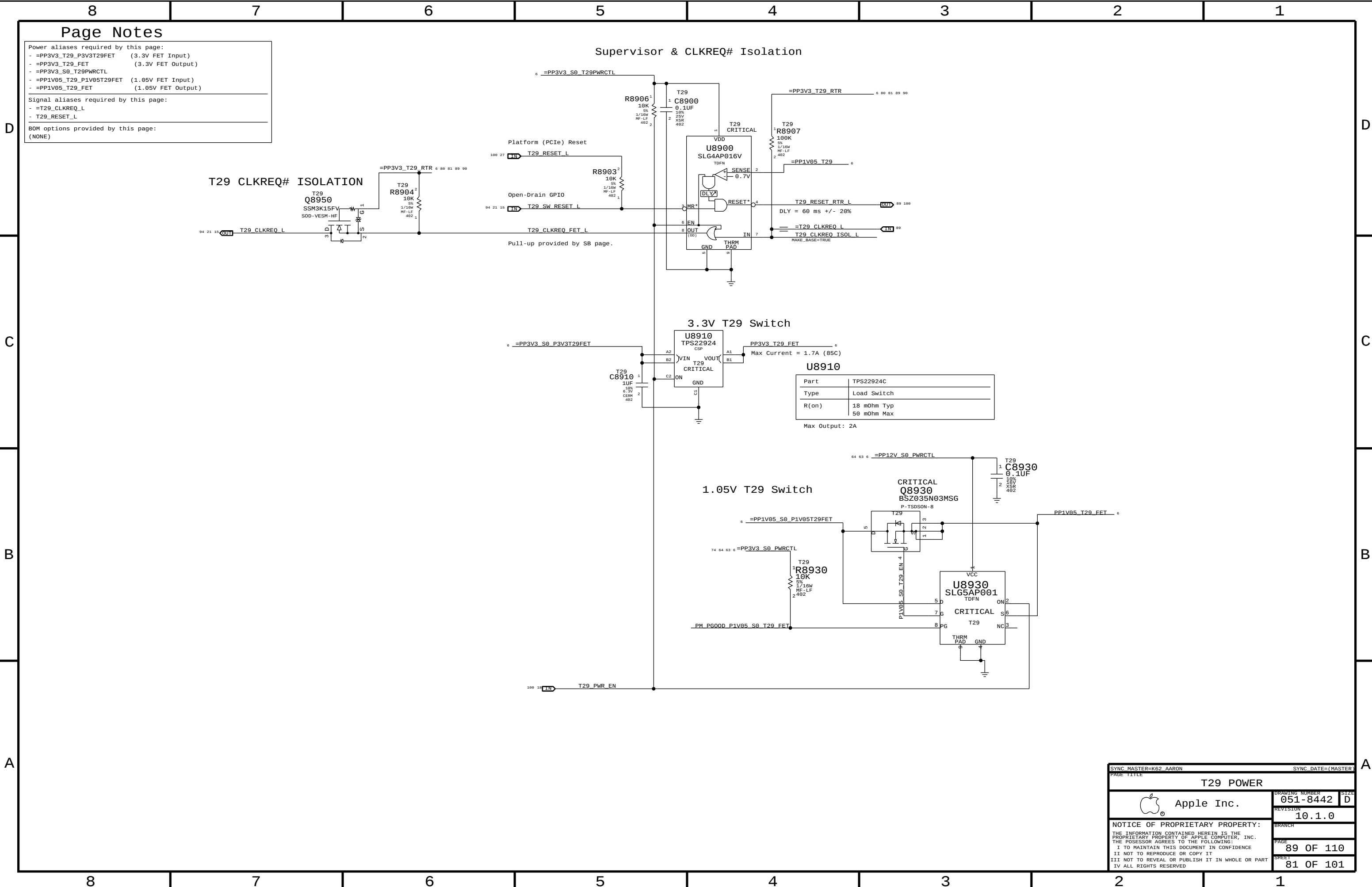
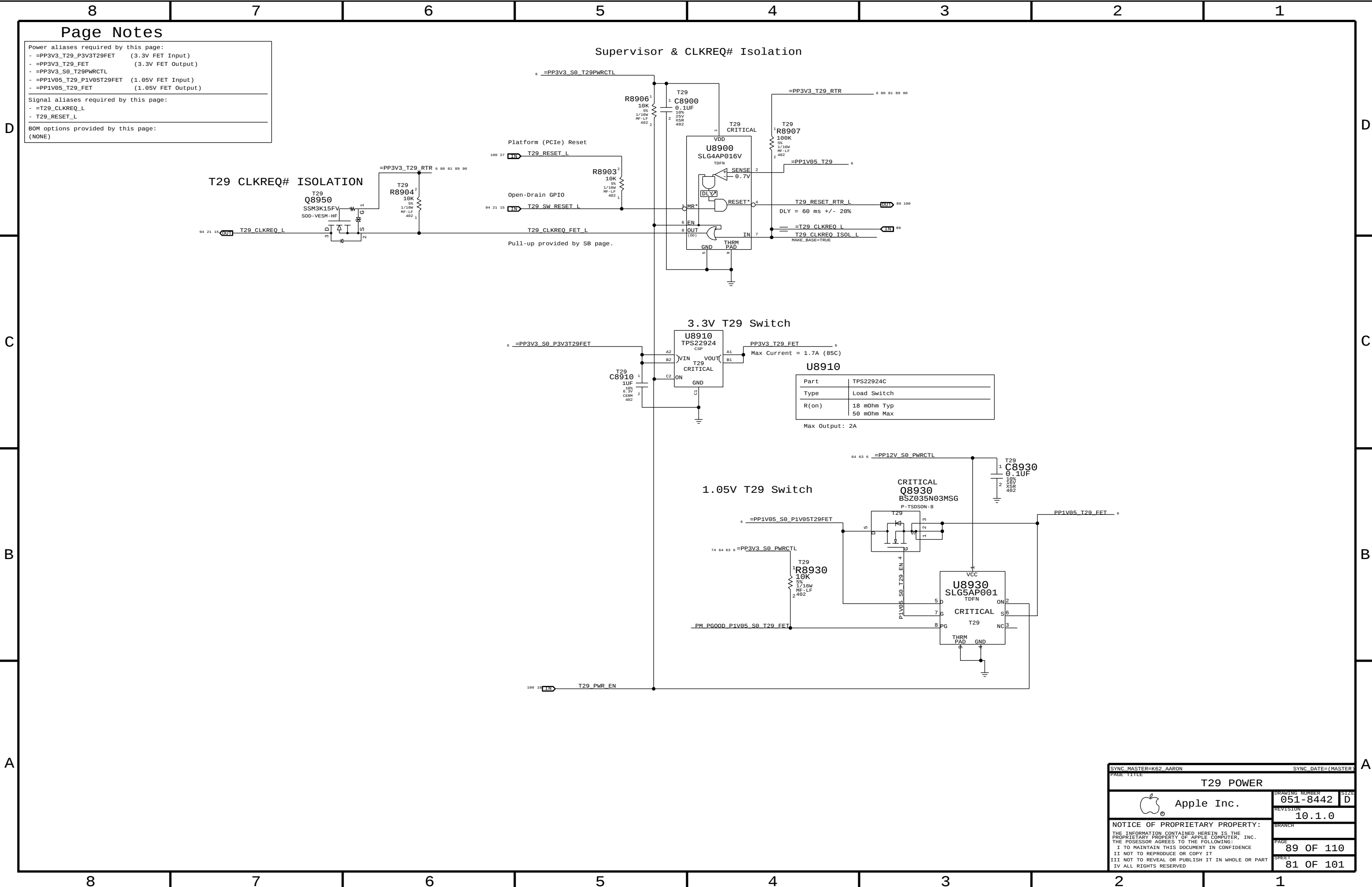
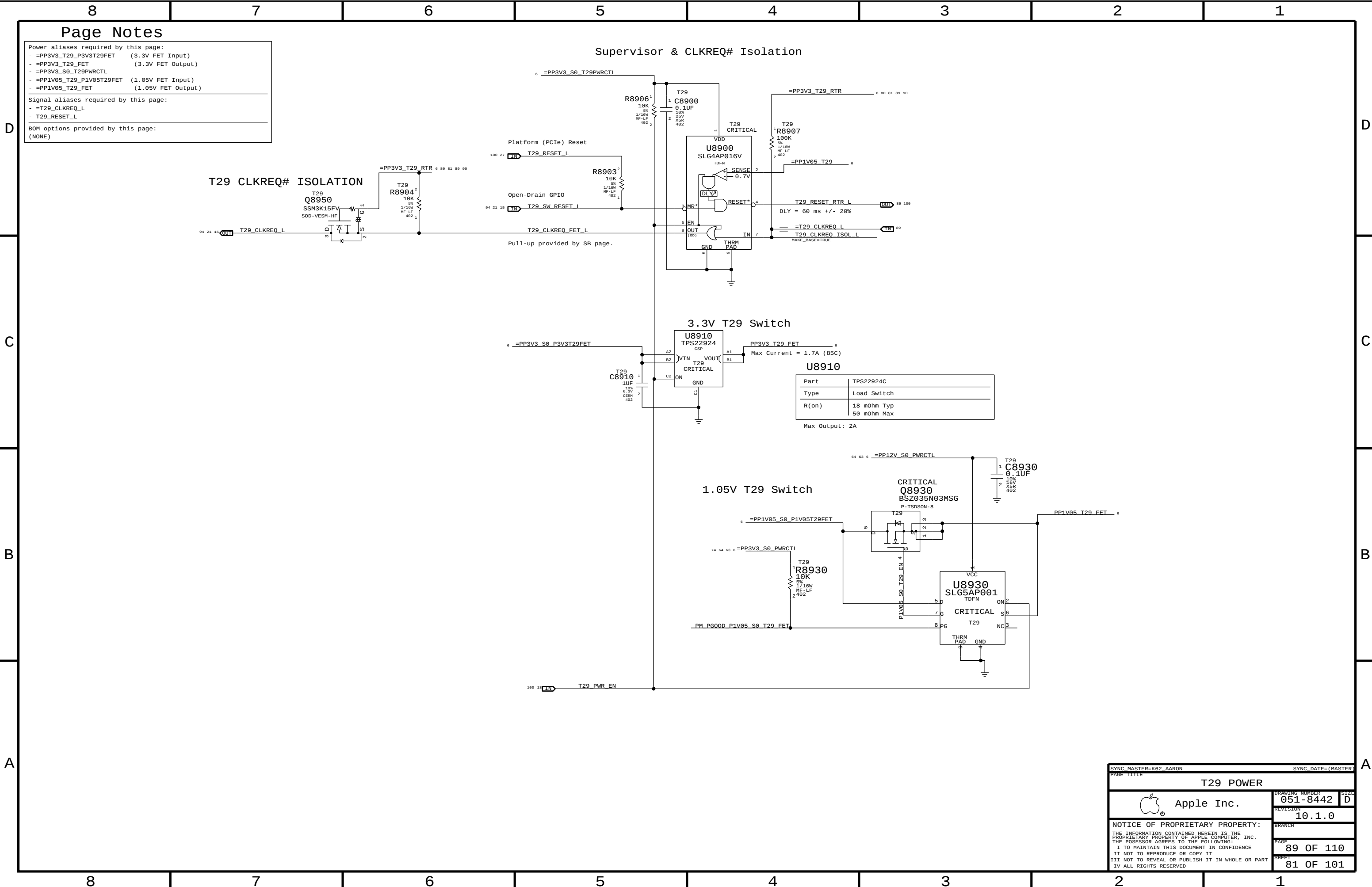
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8 7 6 5 4 3 2 1

Page Notes

Power aliases required by this page:

- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWCTRL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

Signal aliases required by this page:

- =T29_CLKREQ_L
- T29_RESET_L

BOM options provided by this page:

(NONE)

Supervisor & CLKREQ# Isolation

T29 CLKREQ# ISOLATION

Platform (PCIe) Reset

Open-Drain GPIO

T29_CLKREQ FET L

Pull-up provided by SB page.

3.3V T29 Switch

1.05V T29 Switch

T29 PWR_EN

T29

Q8950

SSM3K15FV

SOD-VESM-HF

R8904

10K

5% 1/16W NF-LF 402

R8906

10K

5% 1/16W NF-LF 402

R8907

100K

5% 1/16W NF-LF 402

R8903

10K

5% 1/16W NF-LF 402

C8900

0.1uF

18V XSR 402

C8910

1uF

10% 6.3V CERM 402

U8900

SLG4AP016V

TDFH

U8910

TPS22924

CSP

U8930

SLG5AP001

TDFN

Q8930

BSZ035N03MSG

P-TSDSON-8

PP3V3_T29_RTR

PP1V05_T29

T29_RESET_RTR_L

T29_CLKREQ L

T29_CLKREQ ISOL L

MAKE_BASE=TRUE

PP3V3_S0_P3V3T29FET

PP3V3_T29_FET

Max Current = 1.7A (85C)

U8910

Part

TPS22924C

Type

Load Switch

R(on)

18 mOhm Typ

50 mOhm Max

Max Output: 2A

PP12V_S0_PWCTRL

PP1V05_S0_P1V05T29FET

PP3V3_S0_PWCTRL

PP1V05_T29_FET

PM_PG00D_P1V05_S0_T29_FET

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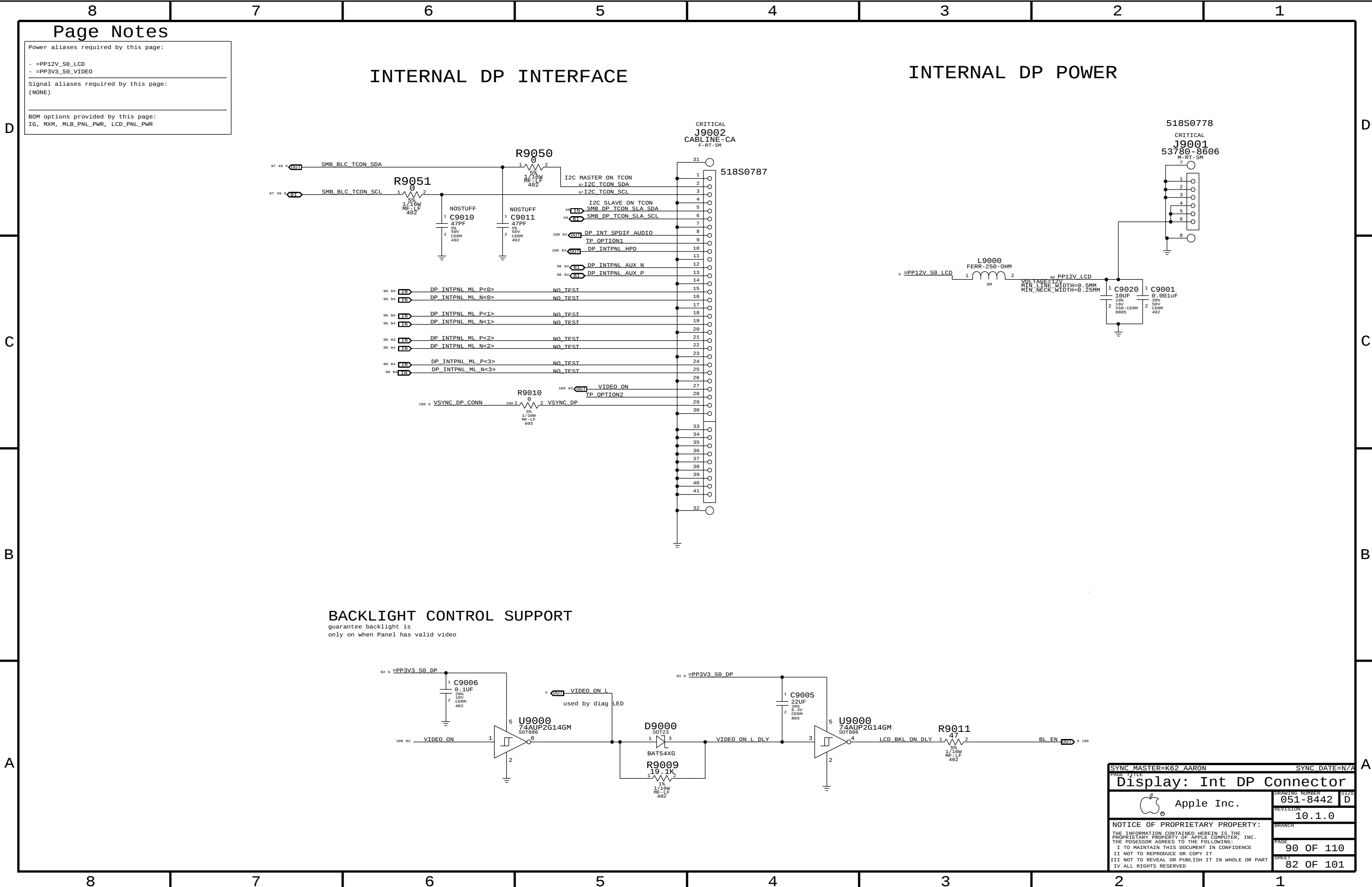
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Page Notes

Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE

INTERNAL DP POWER

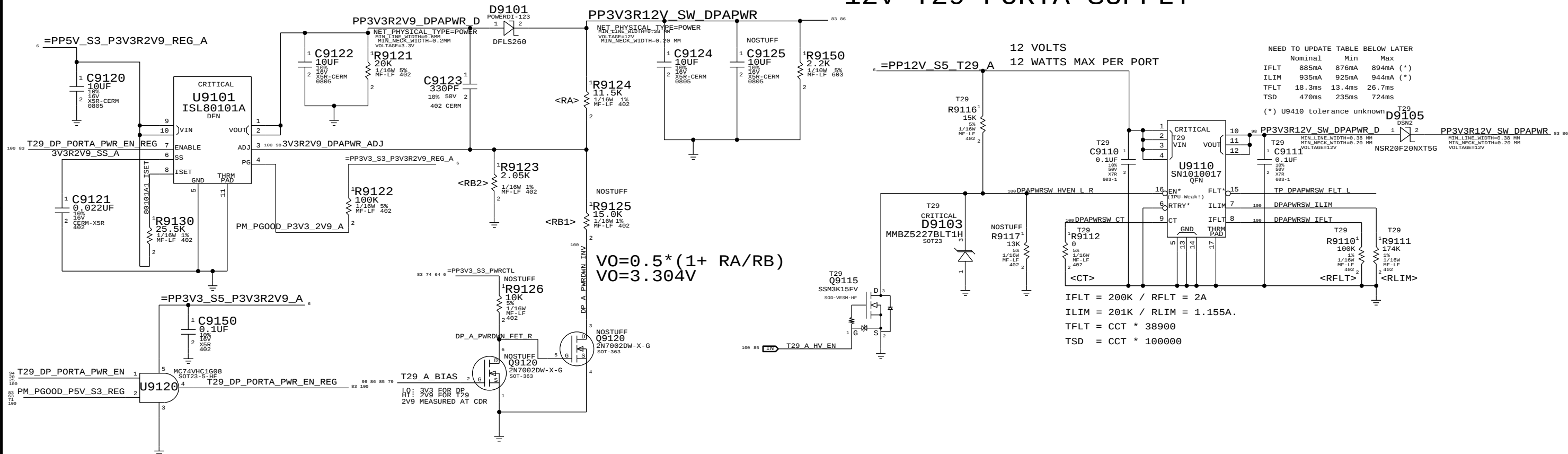
BACKLIGHT CONTROL SUPPORT

guarantee backlight is
only on when Panel has valid video

PAGE 1/1 TITLE		SYNC DATE=N/A	
Display: Int DP Connector		DRAWING NUMBER	051-8442
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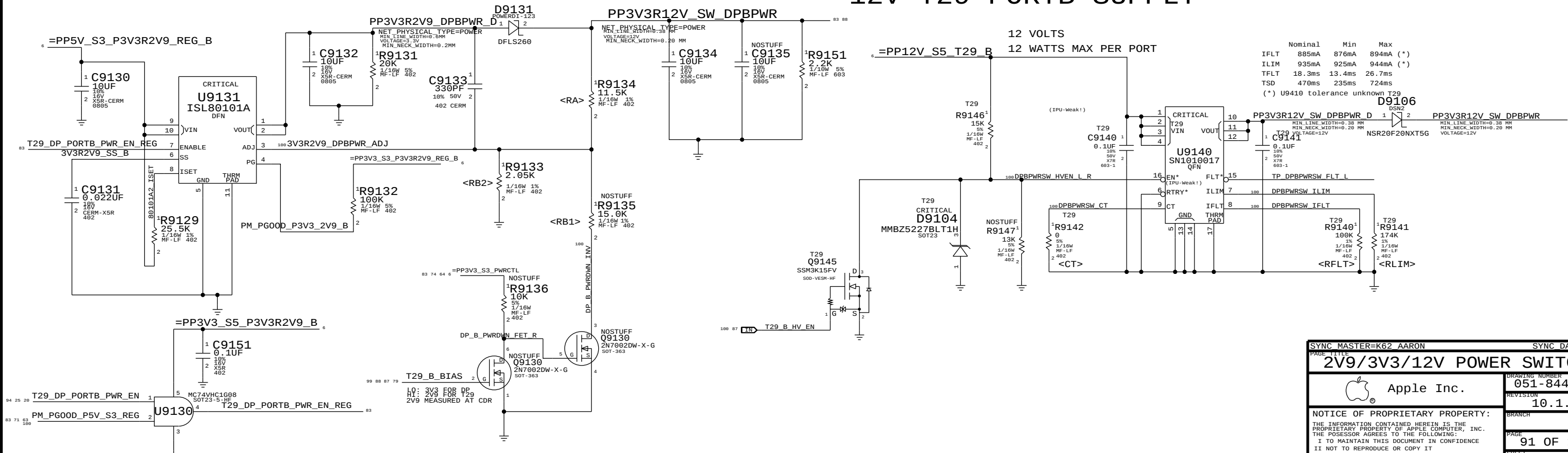
3V3(DP)/2V9(T29) PORTA SUPPLY

12V T29 PORTA SUPPLY

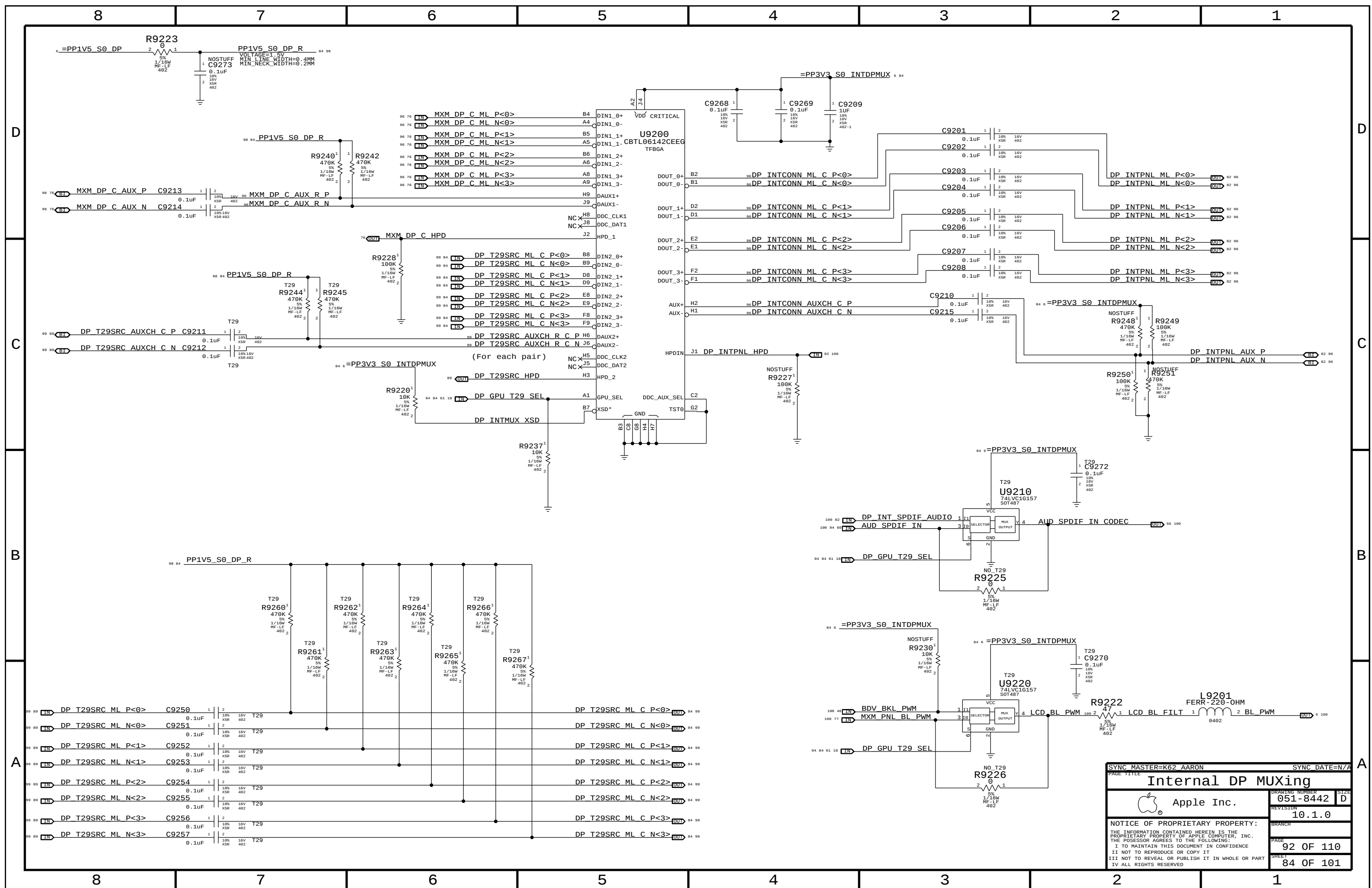


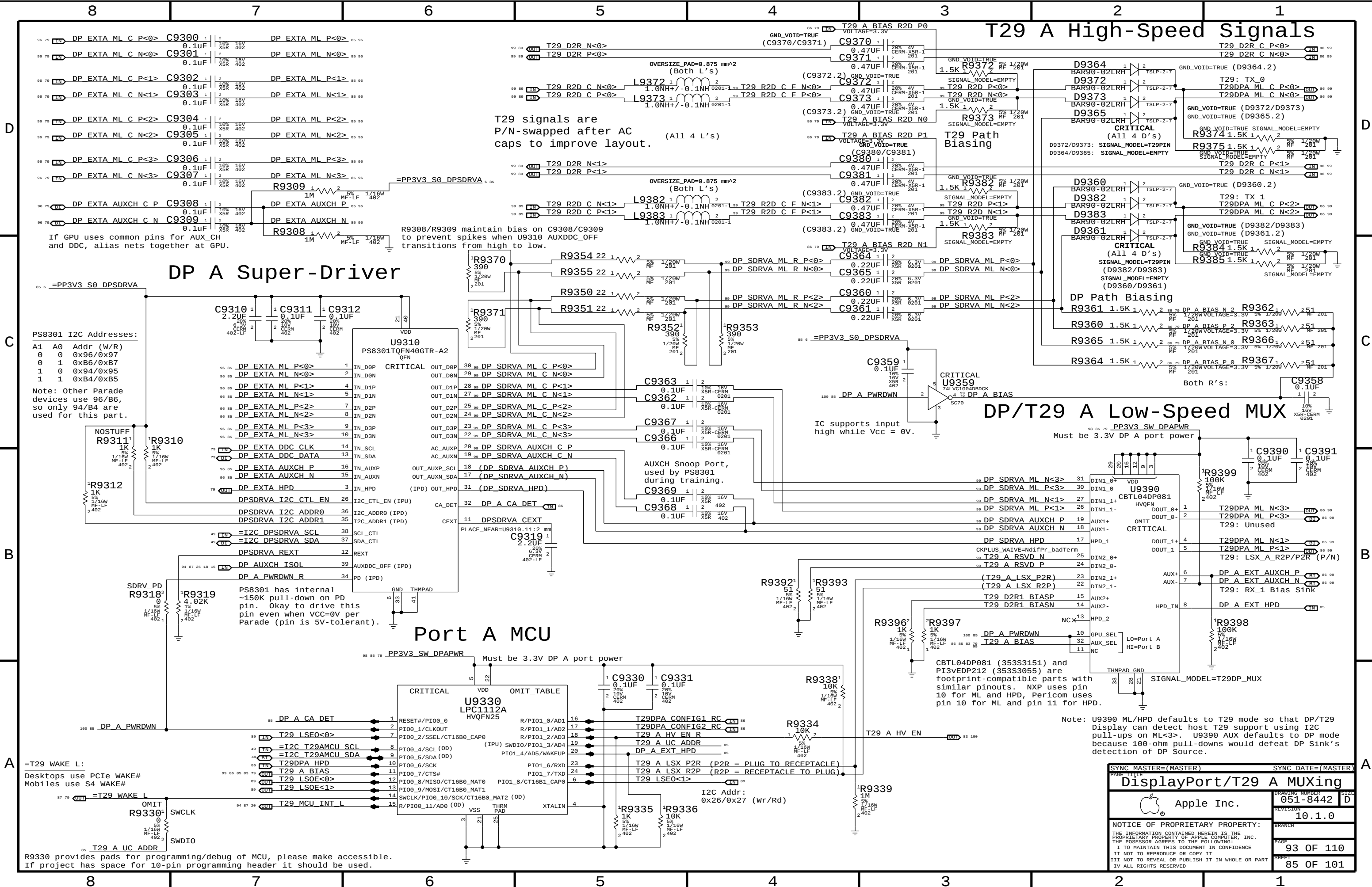
3V3(DP)/2V9(T29) PORTB SUPPLY

12V T29 PORTB SUPPLY



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PAGE TITLE		2V9/3V3/12V POWER SWITCH	
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D

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SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
PAGE TITLE			
DisplayPort/T29 A MUXing			
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		SIZE	D
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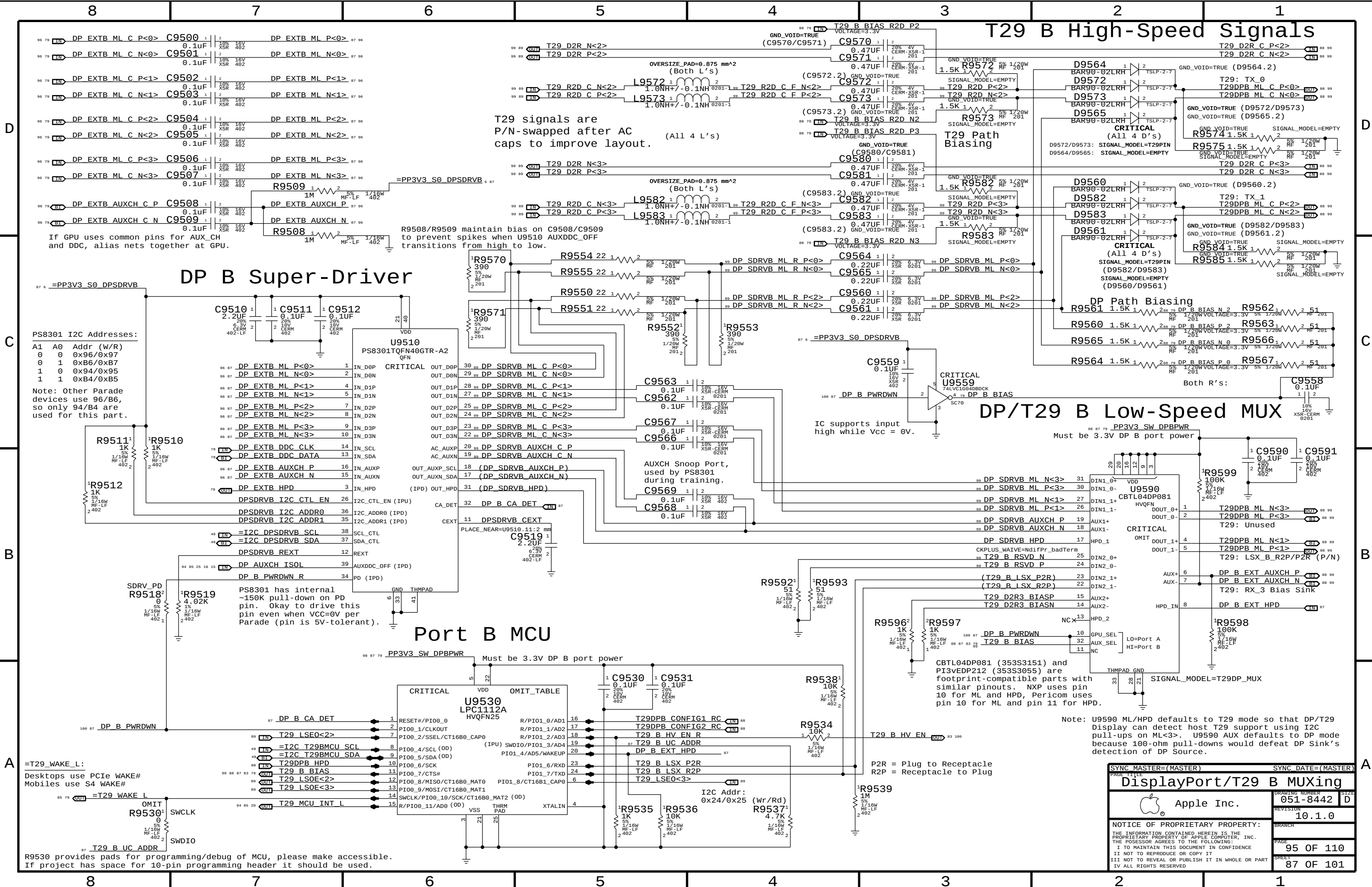


A



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	7	6	5	4	3	2	1
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D

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T29 B High-Speed Signals

DP B Super-Driver

DP/T29 B Low-Speed MUX

Port B MCU

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

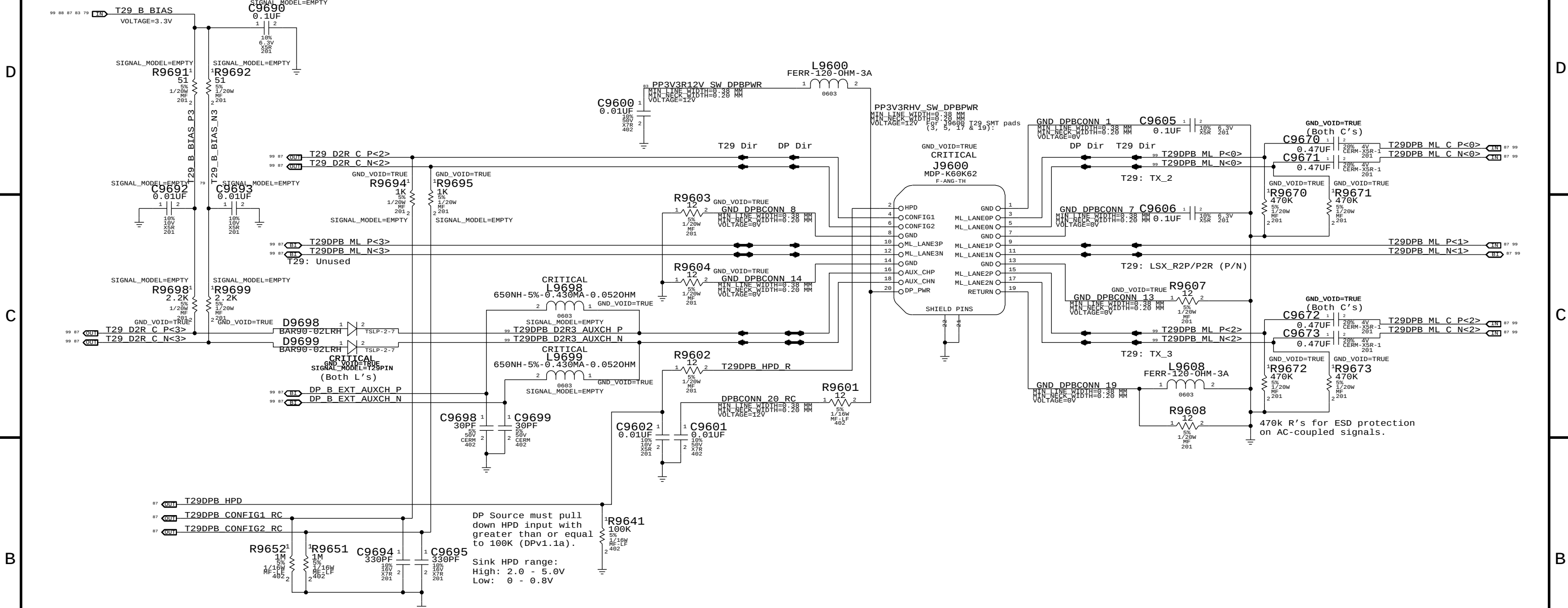
R9530 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

IC supports input high while Vcc = 0V.

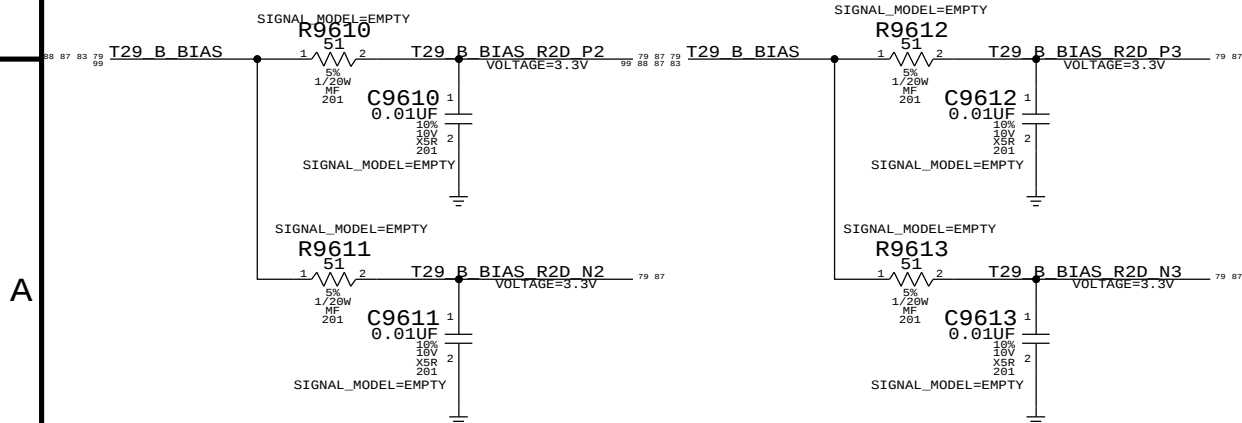
Note: U9590 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9590 AUX defaults to DP mode because 100-ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC MASTER=(MASTER)		SYNC DATE=(MASTER)	
DisplayPort/T29 B MUXing			
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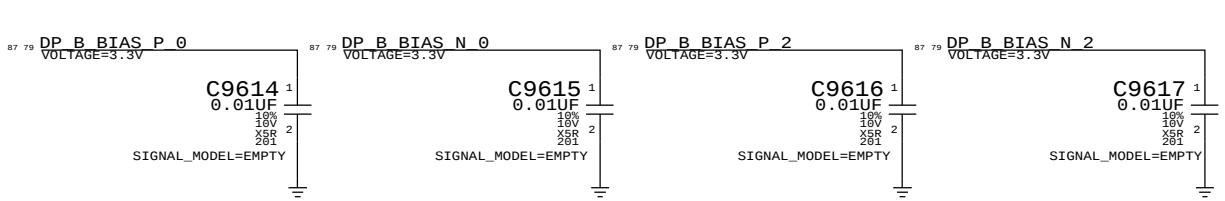
DisplayPort/T29 B Connector



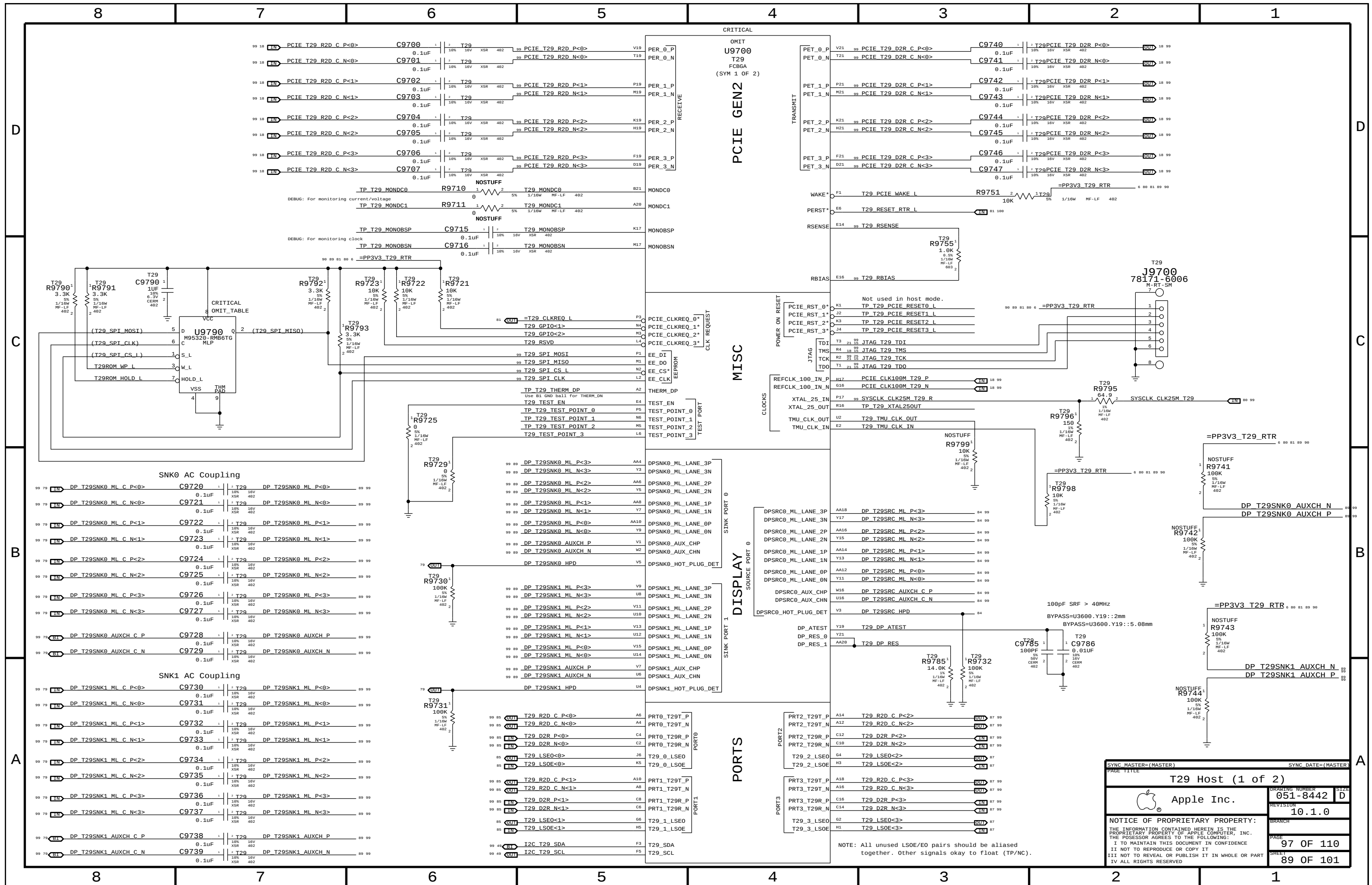
T29 BIAS RC

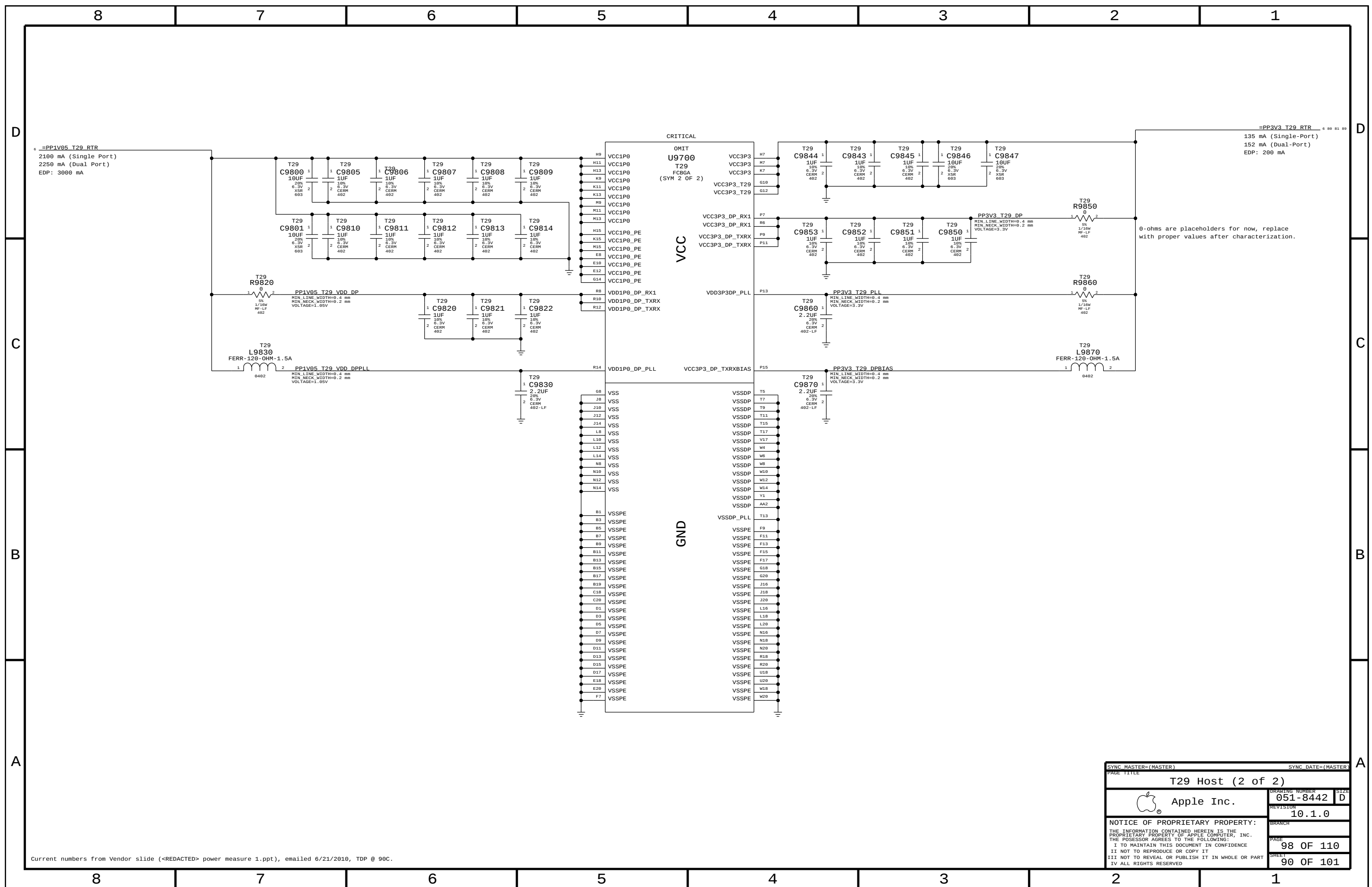


DP BIAS CAPS



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Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
	MEM_68D	MEM_CLK	MEM B CLK P<3..0>	12 32
	MEM_68D	MEM_CLK	MEM B CLK N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM B CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM B CS L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM B ODT<3..0>	12 31
	MEM_34S	MEM_CMD	MEM B A<15..0>	12 31
	MEM_34S	MEM_CMD	MEM B BA<2..0>	12 31
	MEM_34S	MEM_CMD	MEM B RAS L	12 31
	MEM_34S	MEM_CMD	MEM B CAS L	12 31
	MEM_34S	MEM_CMD	MEM B WE L	12 31
	MEM_42S	MEM_DQ_BYTE0	MEM B DQ<7..0>	12 32
	MEM_42S	MEM_DQ_BYTE1	MEM B DQ<15..8>	12 32
	MEM_42S	MEM_DQ_BYTE2	MEM B DQ<23..16>	12 32
	MEM_42S	MEM_DQ_BYTE3	MEM B DQ<31..24>	12 32
	MEM_42S	MEM_DQ_BYTE4	MEM B DQ<39..32>	12 32
	MEM_42S	MEM_DQ_BYTE5	MEM B DQ<47..40>	12 32
	MEM_42S	MEM_DQ_BYTE6	MEM B DQ<55..48>	12 32
	MEM_42S	MEM_DQ_BYTE7	MEM B DQ<63..56>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<0>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<0>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<1>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<1>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<2>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<2>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<3>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<3>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<4>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<4>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<5>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<5>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<6>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<6>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS P<7>	12 32
	MEM_42S_D	MEM_DQS	MEM B DQS N<7>	12 32

MEMORY MISC PROPERTIES

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
MEM_POWER	*	=3:1_SPACING	?

87654321

SYNC_MASTER=K62 ROSITA SYNC_DATE=01/09/2011

Memory Constraints

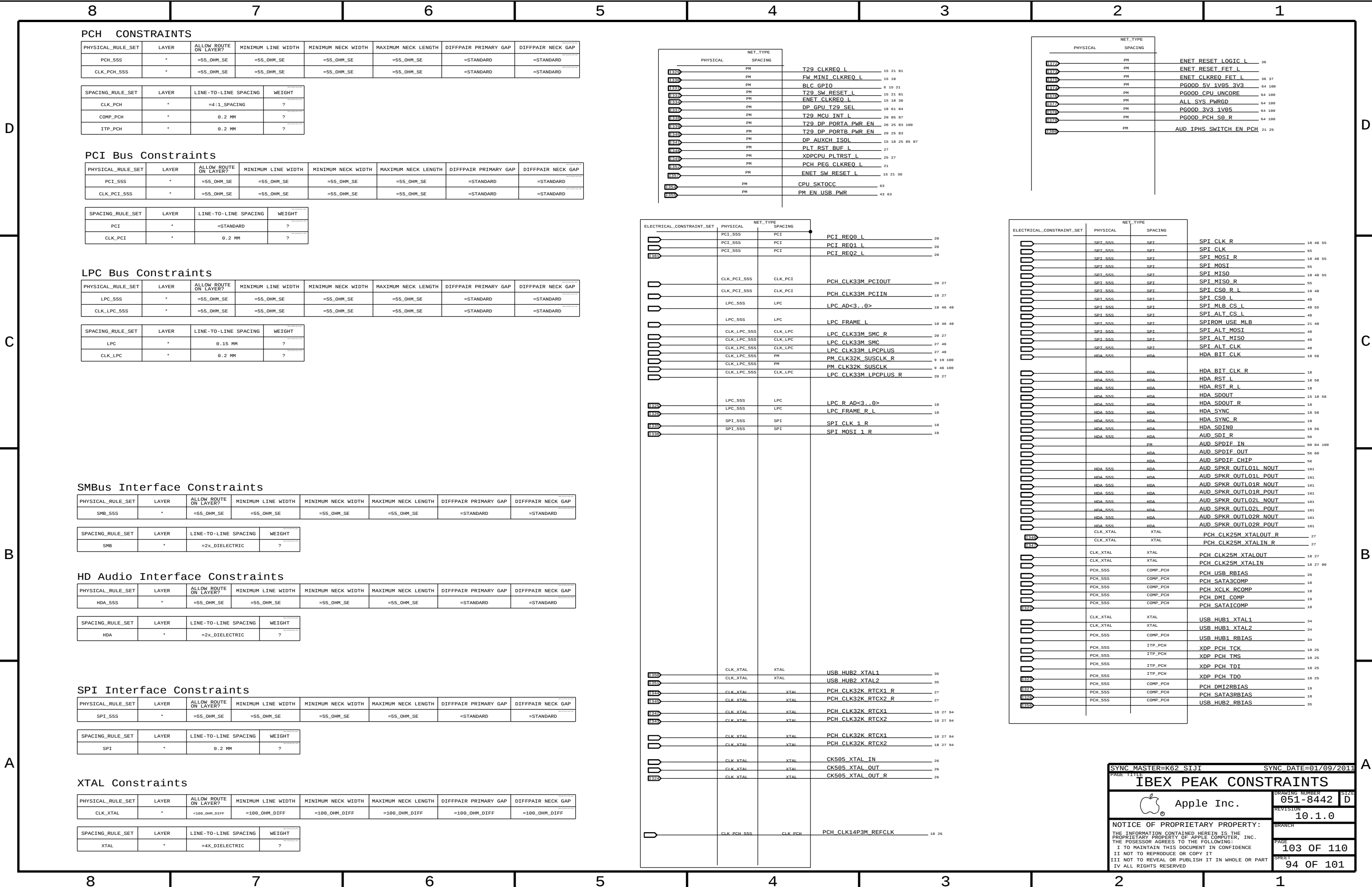
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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
CLK_PCH	*	=4:1_SPACING	?
COMP_PCH	*	0.2 MM	?
ITP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SMB	*	=2X_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
HDA	*	=2X_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

NET_TYPE	PHYSICAL	SPACING
PM	T29_CLKREQ_L	15 21 81
PM	FW_MINI_CLKREQ_L	15 18
PM	BLC_GPIO	6 15 21
PM	T29_SW_RESET_L	15 21 81
PM	ENET_CLKREQ_L	15 18 36
PM	DP_GPU_T29_SEL	18 61 84
PM	T29_MCU_INT_L	20 85 87
PM	T29_DP_PORTA_PWR_EN	20 25 83 100
PM	T29_DP_PORTB_PWR_EN	20 25 83
PM	DP_AUXCH_ISOL	15 18 25 85 87
PM	PLT_RST_BUF_L	27
PM	XDPCPU_PLTRST_L	25 27
PM	PCH_PEG_CLKREQ_L	21
PM	ENET_SW_RESET_L	15 21 36
PM	CPU_SKTOCC	63
PM	PM_EN_USB_PWR	43 63

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	PCI_55S	PCI	PCI REQ0_L 20
	PCI_55S	PCI	PCI REQ1_L 20
	PCI_55S	PCI	PCI REQ2_L 20
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT 20 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIIN 18 27
	LPC_55S	LPC	LPC_AD<3..0> 18 46 48
	LPC_55S	LPC	LPC_FRAME_L 18 46 48
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 20 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 27 46
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 27 48
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R 9 19 100
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK 9 46 100
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R 20 27
	LPC_55S	LPC	LPC_R_AD<3..0> 18
	LPC_55S	LPC	LPC_FRAME_R_L 18
	SPI_55S	SPI	SPI_CLK_1_R 18
	SPI_55S	SPI	SPI_MOSI_1_R 18
	CLK_XTAL	XTAL	USB_HUB2_XTAL1 35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2 35
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1_R 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1 18 27 94
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2 18 27 94
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1 18 27 94
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2 18 27 94
	CLK_XTAL	XTAL	CK505_XTAL_IN 26
	CLK_XTAL	XTAL	CK505_XTAL_OUT 26
	CLK_XTAL	XTAL	CK505_XTAL_OUT_R 26
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK 18 26

NET_TYPE	PHYSICAL	SPACING
PM	ENET_RESET_LOGIC_L	36
PM	ENET_RESET_FET_L	
PM	ENET_CLKREQ_FET_L	36 37
PM	PGOOD_5V_1V05_3V3	64 100
PM	PGOOD_CPU_UNCORE	64 100
PM	ALL_SYS_PMRGD	64 100
PM	PGOOD_3V3_1V05	64 100
PM	PGOOD_PCH_S0_R	64 100
PM	AUD_IPHS_SWITCH_EN_PCH	21 25

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
	SPT_55S	SPT	SPI_CLK_R 18 48 55
	SPT_55S	SPT	SPI_CLK 55
	SPT_55S	SPT	SPI_MOSI_R 18 48 55
	SPT_55S	SPT	SPI_MOSI 55
	SPT_55S	SPT	SPI_MISO 18 48 55
	SPT_55S	SPT	SPI_MISO_R 55
	SPT_55S	SPT	SPI_CS0_R_L 18 48
	SPT_55S	SPT	SPI_CS0_L 48
	SPT_55S	SPT	SPI_MLB_CS_L 48 55
	SPT_55S	SPT	SPI_ALT_CS_L 48
	SPT_55S	SPT	SPIROM_USE_MLB 21 48
	SPT_55S	SPT	SPI_ALT_MOSI 48
	SPT_55S	SPT	SPI_ALT_MISO 48
	SPT_55S	SPT	SPI_ALT_CLK 48
	HDA_55S	HDA	HDA_BIT_CLK 18 56
	HDA_55S	HDA	HDA_BIT_CLK_R 18
	HDA_55S	HDA	HDA_RST_L 18 56
	HDA_55S	HDA	HDA_RST_R_L 18
	HDA_55S	HDA	HDA_SDOOUT 15 18 56
	HDA_55S	HDA	HDA_SDOOUT_R 18
	HDA_55S	HDA	HDA_SYNC 18 56
	HDA_55S	HDA	HDA_SYNC_R 18
	HDA_55S	HDA	HDA_SDI0 18 56
	HDA_55S	HDA	AUD_SDI_R 56
		PM	AUD_SPDIF_IN 66 84 100
		HDA	AUD_SPDIF_OUT 56 60
		HDA	AUD_SPDIF_CHIP 56
	HDA_55S	HDA	AUD_SPKR_OUTL01L_NOUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL01L_POUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL01R_NOUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL01R_POUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL02L_NOUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL02L_POUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL02R_NOUT 101
	HDA_55S	HDA	AUD_SPKR_OUTL02R_POUT 101
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT_R 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN_R 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT 18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN 18 27 80
	PCH_55S	COMP_PCH	PCH_USB_RBIA5 20
	PCH_55S	COMP_PCH	PCH_SATA3COMP 18
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP 18
	PCH_55S	COMP_PCH	PCH_DMI_COMP 19
	PCH_55S	COMP_PCH	PCH_SATA1COMP 18
	CLK_XTAL	XTAL	USB_HUB1_XTAL1 34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2 34
	PCH_55S	COMP_PCH	USB_HUB1_RBIA5 34
	PCH_55S	ITP_PCH	XDP_PCH_TCK 18 25
	PCH_55S	ITP_PCH	XDP_PCH_TMS 18 25
	PCH_55S	ITP_PCH	XDP_PCH_TDI 18 25
	PCH_55S	ITP_PCH	XDP_PCH_TDO 18 25
	PCH_55S	COMP_PCH	PCH_DMI2RBIA5 19
	PCH_55S	COMP_PCH	PCH_SATA3RBIA5 18
	PCH_55S	COMP_PCH	USB_HUB2_RBIA5 35

SYNC MASTER=K62 SIJI

SYNC DATE=01/09/2011

IBEX PEAK CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8442

REVISION 10.1.0

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UNUSED VIDEO NET PHYSICAL CONSTRAINTS

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PAGE TITLE			
GRAPHICS CONSTRAINTS			
 Apple Inc.		DRAWING NUMBER	D
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T29 ELECTRICAL ROUTES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29	*	=5X_DIELECTRIC	?	T29	TOP, BOTTOM	=7X_DIELECTRIC	?

T29 PCI-EXPRESS (SAME RULE AS PCIE)

T29 SPI INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	0.2 MM	?

T29 XTAL CONSTRAINTS

[illegible]

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_XTAL	*	=4X_DIELECTRIC	?

T29 SMBUS INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SMB	*	=2X_DIELECTRIC	?

GREEN CLOCK CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_25M	*	=5X_DIELECTRIC	?

T29 BIAS CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_COMP	*	0.2 MM	?

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		PHYSICAL	SPACING	
	NO TEST=TRUE	T29_900	T29	T29 R2D C P<3..0> 85 87 89
	NO TEST=TRUE	T29_900	T29	T29 R2D C N<3..0> 85 87 89
	NO TEST=TRUE	T29_900	T29	T29 D2R C P<3..0> 86 87 88
	NO TEST=TRUE	T29_900	T29	T29 D2R C N<3..0> 85 86 87 88
	NO TEST=TRUE	T29_900	T29	T29 R2D P<3..0> 85 87
	NO TEST=TRUE	T29_900	T29	T29 R2D N<3..0> 85 87
	NO TEST=TRUE	T29_900	T29	T29 D2R P<3..0> 85 87 89
	NO TEST=TRUE	T29_900	T29	T29 D2R N<3..0> 85 87
	NO TEST=TRUE	T29_900	T29	T29 R2D C F P<3..0> 85 87
	NO TEST=TRUE	T29_900	T29	T29 R2D C F N<3..0> 85 87
	NO TEST=TRUE	T29_900	T29	T29DPA ML P<3..0> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPA ML N<3..0> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPB ML P<3..0> 87 88
	NO TEST=TRUE	T29_900	T29	T29DPB ML N<3..0> 87 88
	NO TEST=TRUE	T29_900	T29	DP A EXT AUXCH P 85 86
	NO TEST=TRUE	T29_900	T29	DP A EXT AUXCH N 85 86
	NO TEST=TRUE	T29_900	T29	DP SDRVA AUXCH C P 85
	NO TEST=TRUE	T29_900	T29	DP SDRVA AUXCH C N 85
	NO TEST=TRUE	T29_900	T29	DP SDRVB AUXCH C P 87
	NO TEST=TRUE	T29_900	T29	DP SDRVB AUXCH C N 87
	NO TEST=TRUE	T29_900	T29	DP B EXT AUXCH P 86 88
	NO TEST=TRUE	T29_900	T29	DP B EXT AUXCH N 87
	NO TEST=TRUE	T29_900	T29	T29DPA D2R1 AUXCH P 86
	NO TEST=TRUE	T29_900	T29	T29DPA D2R1 AUXCH N 86
	NO TEST=TRUE	T29_900	T29	T29DPB D2R3 AUXCH P 88
	NO TEST=TRUE	T29_900	T29	T29DPB D2R3 AUXCH N 88
	NO TEST=TRUE	T29_900	T29	T29DPA ML C N<0> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPA ML C P<0> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPA ML C N<2> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPA ML C P<2> 85 86
	NO TEST=TRUE	T29_900	T29	T29DPB ML C N<0> 87 88
	NO TEST=TRUE	T29_900	T29	T29DPB ML C P<0> 87 88
	NO TEST=TRUE	T29_900	T29	T29DPB ML C N<2> 87 88
	NO TEST=TRUE	T29_900	T29	T29DPB ML C P<2> 87 88
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 R2D P<3..0> 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 R2D N<3..0> 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 R2D C P<3..0> 18 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 R2D C N<3..0> 18 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 D2R P<3..0> 18 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 D2R N<3..0> 18 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 D2R C P<3..0> 18 89
	NO TEST=TRUE	PCIE_850	PCIE	PCIE T29 D2R C N<3..0> 18 89
	NO TEST=TRUE	CLK_PCIE_900	CLK_PCIE	PCIE CLK100M T29 P 18 89
	NO TEST=TRUE	CLK_PCIE_900	CLK_PCIE	PCIE CLK100M T29 N 18 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC ML C P<3..0> 84
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC ML C N<3..0> 84
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC ML P<3..0> 84 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC ML N<3..0> 84 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 ML P<3..0> 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 ML N<3..0> 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 AUXCH P 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 AUXCH N 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 ML C P<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 ML C N<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK0 AUXCH C N 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 ML P<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 ML N<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 AUXCH P 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 AUXCH N 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 ML C P<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 ML C N<3..0> 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 AUXCH C P 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SNK1 AUXCH C N 79 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC AUXCH R C P 84
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC AUXCH R C N 84
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC AUXCH C P 84 89
	NO TEST=TRUE	DP_850	DISPLAYPORT	DP T29SRC AUXCH C N 84 89
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA AUXCH P 89
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA AUXCH N 89
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB AUXCH P 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB AUXCH N 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML C P<3..0> 85
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML C N<3..0> 85
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML P<3..0> 85 89
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML N<3..0> 85
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML R P<3..0> 85
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVA ML R N<3..0> 85
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML C P<3..0> 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML C N<3..0> 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML P<3..0> 87 89
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML N<3..0> 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML R P<3..0> 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	DP SDRVB ML R N<3..0> 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	T29 A RSVD P 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	T29 B RSVD N 87
	NO TEST=TRUE	T29_900	DISPLAYPORT	T29 B RSVD P 87

T29 NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
	PHYSICAL	SPACING		
	T29_SPT_55S	T29_SPT	JTAG T29 TDI	15 21 89
	T29_SPT_55S	T29_SPT	JTAG T29 TMS	15 18 89
	T29_SPT_55S	T29_SPT	JTAG T29 TCK	15 21 25
	T29_SPT_55S	T29_SPT	JTAG T29 TDO	15 21 89
IE5V	T29_SPT_55S	T29_SPT	T29 SPI MOSI	89
IE40	T29_SPT_55S	T29_SPT	T29 SPI MISO	89
IE80	T29_SPT_55S	T29_SPT	T29 SPI CS_L	89
IE40	T29_SPT_55S	T29_SPT	T29 SPI CLK	89
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	89 89 99
	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29_R	89 99
	T29_SMB_55S	T29_SMB	I2C T29_SDA	49 89
	T29_SMB_55S	T29_SMB	I2C T29_SCL	49 89
IE20	CLK_25M_55S	CLK_25M	SYSCLK CLK25M_SB	89
IE20	CLK_25M_55S	CLK_25M	SYSCLK CLK25M_ENET	89
IE20	CLK_25M_55S	CLK_25M	ENET CLK25M_XTALI_QSC	36 89
IE20	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29_CLK	89
IE80	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29	89 89 99
IE20	CLK_25M_55S	CLK_25M	SYSCLK CLK25M T29_R	89 99
IE20	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X2	89 99
IE80	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X2_R	89
IE20	T29_XTAL_100D	T29_XTAL	SYSCLK CLK25M_X1	89
IE80	T29_55S	T29_COMP	T29_RSENSE	89
IE20	T29_55S	T29_COMP	T29_RBIA5	89
IE80	T29_COMP	T29_COMP	T29_A_BIAS	79 83 85 86
IE80	T29_COMP	T29_COMP	T29_B_BIAS	79 83 87 88
IE40	T29_COMP	T29_COMP	DP_A_BIAS	79 85

PM NET PROPERTIES
(PM, RESET, EN, PG00D)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

NET_TYPE		PHYSICAL	SPACING		
PHYSICAL	SPACING				
PM				4V5_REG_EN	56
PM				3V42G3H_SHDN_L	73
PM				ALL_SYS_PWRGD_R	5 32 64
PM				ALL_SYS_PWRGD_SMC	46 64
PM				AP_PWR_EN	20 25 33
PM				AP_MINI_RESET_L	33
PM				AUD_I2C_INT_L	20 62
PM				AUD_IP_PERIPHERAL_DET	20 61
PM				AUD_IPHS_SWITCH_EN	21 62
PM				AUD_SPDIF_IN	60 84 94
PM				AUD_SPDIF_IN_CODEC	56 84
PM				BDV_BKL_PWM	46 84 100
PM				BL_PWM	6 84
PM				BL_EN	6 82
PM				BDV_BKL_PWM	46 84 100
PM				CK505_27MHZ_EN	26
PM				CPUVTT_REG_EN	63
PM_VTT				CPUVTT_REG_PG00D_R	63
PM				CPU_MEM_RESET_L	11 32
PM				CPU_PECI_R	46
PM_VTT				CPU_PWRGD	11 21 25
PM				CPU_RESET_L	11 27
PM				CPU_SKTOCC_L	11 63
PM				CPU_CATERR_L	11
PM				CPU_PECI	11 21 46
PM				CPU_PROCHOT_L	11 47 65
PM				CPU_THRMTRIP_L	11 47
PM				CPU_PROC_SEL	11 19
PM				DEBUG_RESET_L	27 48
PM				DDRVTT_EN	82 84
PM				DP_INT_SPDIF_AUDIO	82 84
PM				DP_INTPNL_HPD	82 84
PM				3V3R2V9_DPAPWR_ADJ	83 98
PM				DP_A_PWRDWN	83
PM				DP_A_PWRDWN_FET_R	83
PM				DP_A_PWRDWN_INV	83
PM				DPAPWRSW_HVEN_L_R	83
PM				DPAPWRSW_CT	83
PM				DPAPWRSW_ILIM	83
PM				DPAPWRSW_IFLT	83
PM				T29_A_HV_EN	83 85
PM				3V3R2V9_DPBWPR_ADJ	83
PM				DP_B_PWRDWN	87
PM				DP_B_PWRDWN_FET_R	83
PM				DP_B_PWRDWN_INV	83
PM				DPBPWRSW_HVEN_L_R	83
PM				DPBPWRSW_CT	83
PM				DPBPWRSW_ILIM	83
PM				DPBPWRSW_IFLT	83
PM				T29_B_HV_EN	83 87
PM				T29_PWR_EN	18 81 100
PM				T29_RESET_RTR_L	81 89
PM				LCD_BL_FILT	84
PM				LCD_BLK_ON_DLY	84
PM				LCD_BL_PWM	84
PM				MXM_PNL_BL_PWM	77 84

NET_TYPE		PHYSICAL	SPACING		
PHYSICAL	SPACING				
PM				ENET_PWR_EN	20 25 36
PM				ENET_LOW_PWR	15 21 37
PM				FW_RESET_L	27 39
PM				ENET_RESET_L	27 36
PM				FW_PME_L	15 21 39
PM				FW_PWR_EN	15 21
PM				FW_CLKREQ_L	15 39
PM				ISOLATE_CPU_MEM_L	21 25 32
PM				LPC_PWRDWN_L	19 46 48
PM				MEM_RESET_L	30 31 32 92
PM				MINI_CLKREQ_L	15 33
PM				MINI_RESET_L	27 33
PM				MXM_CLKREQ_L	9 76
PM				MXM_GOOD	5 21 25
PM				ODD_PWR_EN_L	15 21 42
PM				RTC_RESET_L	18 27 100
PM				RSMRST_PWRGD	46 64
PM				RTC_RESET_L	18 27 100
PM				S4_ENABLES	63
PM				SDCONN_STATE_RST_L	95
PM				SDCONN_DETECT_BUF_L	20 25 45
PM				SDCARD_RESET	15 21 44 101
PM				SDCARD_RESET_L	44
PM				SDCARD_PLT_RST_L	27 44
PM				SDCARD_PLT_RST_L_R	44
PM				SMC_PM_G2_EN	46 75
PM				SMC_PM_G2_EN_R	75
PM				SMC_PM_G2_EN_L	75
PM				SS_DG_1	75
PM				SS_MSFT_G1	75
PM				USE_HDD_OOB_L	20 51
PM				HDD_OOB_1V00_REF	51
PM				SMC_ADAPTER_EN	19 46 47
PM				SMC_RUNTIME_SCI_L	21 46 47
PM				SMC_WAKE_SCI_L	15 18 21 46
PM				SMC_DELAYED_PWRGD	47 64
PM				SMC_LRESET_L	27 46
PM				SMC_RESET_L	46 47 48
PM				SMC_PROCHOT	46 47
PM				SMC_PROCHOT_3_3_L	46 47
PM				SMC_ONOFF_L	46 47
PM				SMC_MANUAL_RST_L	47
PM				SPI_DESCRIPTOR_OVERRIDE_L	18 46
PM				T29_PWR_EN	18 81 100
PM				T29_RESET_L	27 81
PM				T29_DP_PORTA_PWR_EN	20 25 83 94
PM				T29_DP_PORTA_PWR_EN_REG	83
PM_VTT				XDP_CPUPWRGD	11 25
PM_VTT				XDP_DBRESET_L	11 25
PM_VTT				XDP_PWRGD	25 27
PM				XDPPCH_PLTRST_L	20 25 34
PM				USB_HUB_SOFT_RESET_L	20 25 34
PM				VSYNC_DP_CONN	6 82
PM				VSYNC_DP	82
PM				VIDEO_ON	62
PM				VTT_REG_PG00D_L	63

NET_TYPE		PHYSICAL	SPACING		
PHYSICAL	SPACING				
PM				PLT_RESET_L	20 27
PM_VTT				PLT_RESET_LS1V05_L	11
PM				PM_BATLOW_L	15 19 40
PM				PM_CLK32K_SUSCLK	9 46 94
PM				PM_CLK32K_SUSCLK_R	9 19 94
PM				PM_CLKRUN_L	15 19 46 48
PM				PM_PWRBTN_L	19 25 46
PM				PM_RSMRST_L	27 46
PM				PM_RSMRST_PCH_L	19 27
PM				PCH_SRTCST_L	18
PM				PCH_INTVRMEN_L	18
PM				PCH_DSWVRMEN	19
PM				PCH_DF_TVS	19
PM				PCH_PROCPWRGD	21
PM				PCIE_WAKE_L	19 33 36 79
PM				PM_DSW_PWRGD	19
PM				PM_ASW_PWRGD	19 64
PM				PM_MEM_PWRGD_R	11
PM				PM_EN_DDR1V5_S3_REG	63 72
PM				PM_EN_DDRVTT_S0_REG	32 63 72
PM				PM_EN_P12V_S0_FET	6 63
PM				PM_EN_P1V05_S0_REG	63 68
PM				PM_EN_P1V05_S3_REG	63 74
PM				PM_EN_P1V5_S0_FET	63 74
PM				PM_EN_P1V8_S0_REG	63 72
PM				PM_EN_P3V3_S0_FET	63 74
PM				PM_EN_P3V3_S3_FET	63 74
PM				PM_EN_P3V3_S5_REG	71
PM				PM_EN_P5V_S0_FET	63 74
PM				PM_EN_P5V_S3_REG	63 71
PM				PM_EN_PVCCSA_S0_REG_L	64
PM				PM_EN_VCCSA_S0_CPU	63 65
PM				PM_EN_PVCORE_CPU	63 65
PM_VTT				PM_MEM_PWRGD	11 19 100
PM				PM_MXM_EN	64 77
PM				PM_PCH_PWRGD_R	64
PM				PM_PECI_PWRGD	46 64
PM				PM_PECI_PWRGD_R	46
PM				PM_PG00D_DDR1V5_S3_REG	5 63 72
PM				PM_PG00D_P1V05_S0_REG	63 64 68
PM				PM_PG00D_P1V5_S0_FET	11 64 74
PM				PM_PG00D_P1V8_S0_REG	64 72
PM				PM_PG00D_P3V3_S0_FET	63 64 74
PM				PM_PG00D_P3V3_S3_FET	34 74
PM				PM_PG00D_P3V3_S5_REG	27 64 71
PM				PM_PG00D_P5V_S0_FET	63 64 74
PM				PM_PG00D_MINI	33
PM				PM_PG00D_PVCORE_CPU	5 25 64 65
PM				PM_PG00D_PVCCSA_S0_REG	63 64
PM				PM_PG00D_P5V_S3_REG	63 71 83
PM				PM_PG00D_PVAXG	5 65
PM_VTT				PM_MEM_PWRGD	11 19 100
PM				PM_MEM_PWRGD_L	11
PM				PM_MXM_PG00D	64 77
PM				PM_PCH_PWRGD	19 21 64
PM				PM_SLP_S3_5V	32
PM				PM_SLP_S3_5V_L	32
PM				PM_SLP_S3_5V_R2	32
PM				PM_SLP_S3_L	5 19 26 32 36 46 47 63
PM				PM_SLP_S4_L	5 19 32 46 47 63 100
PM				PM_SLP_S5_L	5 19 46 47 63
PM_VTT				PM_SYNC	11 19
PM				PM_SYSRST_L	19 25 27 46
PM				PM_SYS_PWRGD	19 32 64
PM_VTT				PM_THRMTRIP_L	21 47
PM				PM_SLP_S3_BUF_L	63
PM				PM_SLP_S4_1_L_R	63
PM				PM_SLP_S4_D_L	32
PM				PM_SLP_S4_L	5 19 32 46 47 63 100
PM				PG00D_P1V5_S0_DLY	11
PM				PG00D_1V8_S0_G1	64
PM				PG00D_1V8_S0_G2	64
PM				PG00D_P12V_S0	63 64
PM				PG00D_P1V8_S0	64
PM				PG00D_PCH_S0	5 64
PM				PG00D_PCH_S0_R	64 94
PM				PG00D_SYSPWR0K	64
PM				PG00D_SYSPWR0K_R	64
PM				POWER_BUTTON_L	47
PM				PEG_RESET_L	9 27
PM				PG00D_CPU_S0	64
PM				PG00D_CPU_UNCORE	64 94
PM				PG00D_5V_1V05_3V3	64 94
PM				PG00D_3V3_1V05	64 94
PM				PG00D_12V_S0_G1	64
PM				PG00D_12V_S0_G2	64
PM				9V_COMP_REF	64
PM				12V_COMP_REF	64
PM				ALL_SYS_PWRGD	64 94

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SYNC DATE=01/09/2011

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